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TO 31S5-2FYQ42-161

OPERATOR, ORGANIZATIONAL, DIRECT SUPPORT,
GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL

# RECEIVER-PHASE COMPARATOR CM-364/G

VLF-12B

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

OCTOBER 1968

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THE NAVY, AND THE AIR FORCE

WASHINGTON, D. C., *14 October 1968*

# Operator, Organizational, Direct Support, General Support, and Depot Maintenance Manual

# RECEIVER-PHASE COMPARATOR CM–364/G

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# CHAPTER 1

# INTRODUCTION

## Section I. GENERAL

### 1-1. Scope

This manual contains operating instructions and maintenance procedures for Receiver-Phase Comparator CM-364/G (hereinafter called the vlf-12B receiver-phase comparator, or simply the vlf-12B), which is a major component of Station Timing Units for Automatic Digital Message Switching Centers AN/FYQ-42(V)1 through AN/FYQ-42(V)12 and AN/FYQ-42(V)T1, which are part of the automatic digital network (AUTODIN). This manual is divided into five chapters. Chapter 1 contains general information and technical characteristics; chapter 2 contains installation procedures and complete operating instructions; chapter 3 describes the principles of operation; chapter 4 provides instructions for maintaining and overhauling the equipment; and chapter 5 explains location of illustrations which support this equipment.

### 1-2. Indexes of Equipment Publications

*a. New Editions, Changes, or Additional Publications.* Determine whether there are any new editions, changes, or additional information pertaining to your equipment by referring to DA Pam 310-4 (Army), NAVSANDA Pub 2002 (Navy), or Numerical Index and Requirement Table T. O. 0-1-01N (Air Force).

*b. Modification Work Orders.* Refer to the latest edition of DA Pam 310-7 to determine whether there are any Modification Work Orders (MWO's) pertaining to the equipment.

### 1-3. Forms and Records

*a. Report of Unsatisfactory Equipment.* Report unsatisfactory equipment in accordance with procedures in TM 38-750 (Army), NW 00-25-546 (Navy), or TO-00-35D-54 (Air Force).

*b. Report of Packaging and Handling Deficiencies.* Fill out and forward DD Form 6 (Report of Packaging and Handling Deficiencies) as prescribed in AR 700-58 (Army), NAVSUP Pub 378 (Navy), or AFR 71-4 (Air Force).

*c. Discrepancy in Shipment Report.* Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38 (Army), NAVSUP Pub 459 (Navy), or AFM 75-34 (Air Force).

*d. Report of Maintenance.* Records and reports of preventive maintenance and repairs must be made in accordance with procedures in TM 38-750 (Army), OPNAV Form 4700, Subject: Planned Maintenance System Feedback Report (Navy), or AFM 66-1 (Air Force).

*e. Report of Equipment Manuals Improvements.* Report of errors, omissions, and recommendations for improving this manual by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to DA Publications) and forwarded to Commanding General, U. S. Army Electronics Command, ATTN: AMSEL-ME-NMP-AD Fort Monmouth, New Jersey 07703 (Army); NAVSHIPS 5600/2 (REV 10-67) (Formerly NAVSHIPS 4914) and forwarded to: Commander, Naval Electronics System Command, ATTN: 0451C, Washington D. C. 20360 (Navy); or AFTO Form 22 (Technical Order System Publications Deficiency Report) and forwarded to: Commander, Oklahoma City Air Materiel Area, ATTN: OCNDT (B-F), Tinker Air Force Base, Ok. 73145 (Air Force).

## Section II. DESCRIPTION AND DATA

### 1-4. Major Components

Table 1-1 of this manual lists the major components, by nomenclature, name, and part number of the vlf-12B receiver-phase comparator, serial numbers 122-132 and 179-180. The items in the part number column followed by an asterisk indicate printed-circuit boards to which changes have been made in the vlf-12B, serial numbers 179-180. All changes have been indicated, as alternates, on the schematics and parts placement diagrams. Table 1-2 lists the differences between circuit boards in serial numbers 122-132 and 179-180.

*Table 1-1. Major Components*

| Nomenclature | Name | Part No. |
|---|---|---|
| A1 | RF Amplifier and First Mixer. | 330039-101 * |
| A2 | IF and AGC Amplifiers. | 200139-101 * |
| A4 | Normal-Mode Second Mixer. | 200151-101 |
| A5 | Three Flip-Flops and Gates. | 200160-101 |
| A6 | Local Oscillator and VCO. | 200163-101 |
| A7 | Mod-10 Counter | 200022-103 |
| A8 | Mod-10 Counter | 200022-103 |
| A9 | Four Flip-Flops | 200016-102 |
| A10 | One-Shot and Reset | 200157-101 |
| A12 | Slow-Loop Synthesizer and Phase Detector. | 200171-101 * |
| A13 | Fast-Loop Synthesizer and Phase Detector. | 200168-101 * |
| A14 | 100-KC Amplifier and Phase Shifter. | 200154-101 * |
| A15 | Servo and AGC Phase Detectors. | 200433-101 * |
| A16 | 1-KC IF Amplifier | 200142-101 |
| A17 | Servo Cutout | 200177-101 * |
| A18 | Servo-Motor Driver | 200174-101 * |
| A19 | Audio Amplifier | 200136-101 * |
| A20 | ± 12-Volt Power Supply. | 200124-101 * |
| A21 | Mod-10 100-KC-to-10-KC Divider. | 200022-103 |
| A22 | Mod-10 10-KC-to-1-KC Divider. | 200022-103 |
| A23 | Mod-10 1-KC-to-100-PPS Divider. | 200022-103 |
| A24 | 76.8-KC-to-100-KC Converter. | 200394-101 |
| A25 | Output Buffers | 200165-101 |
| A27 | Servo Assembly | 300034-101 |
| A28 | CHANNEL SELECTOR Thumbwheel Switches. | 460063-101 |
| L1 | RF Interference Filter | |
| LS1 | Loudspeaker | |
| --- | Chart Recorder | |
| --- | Accessory Kit (Power Cable, Card Extractor, and Card Extender). | |

*See table 1-2.

*Table 1-2. Differences in Circuit Boards*

| Circuit board | Reference des | Serial No. 122-132 | Serial No. 179-180 |
|---|---|---|---|
| A1 | S1R1 | 3480 ohms | 3.3K |
| | S1R3 | 348 ohms | 330 ohms |
| | S1R5 | 34.8 ohms | 33 ohms |
| | S1R7 | 3.48 ohms | 3.3 ohms |
| | S1R9 | 0.5 ohm | 0.51 ohm |
| A2 | R8 | 390 ohms | 180 ohms (sensistor) |
| | R19 | 6.2 K | 3K |
| A12 | Q6 | 2N2222 | 2N3643 |
| A13 | Q7, Q14 | 2N2222 | 2N3643 |
| A14 | L1 | 25 mh | 22 mh |
| A15 | CR4-CR7 | 1N270 | 1N625 |
| | Q1 | 2N1169 | SM8481 |
| | Q2 | 2N1319 | 2N2334 |
| | Q7 | 2N1995 | SM8481 |
| | R16 | 2.2K | 1.6K |

*Table 1-2. Differences in Circuit Boards*—Continued

| Circuit board | Reference des | Serial No. 122-132 | Serial No. 179-180 |
|---|---|---|---|
| | R26 | 21.5K | 20.5K |
| | R28 | 3.6 meg | 2.7 meg |
| A17 | R11 | 3K | 2.7K |
| | R12 | 3K | 1.5K (sensistor) |
| A18 | Q7, Q9 | 2N3638 | 2N4121 |
| | Q8, Q10 | 2N3646 | 2N3567 |
| | R12 | 68 ohms | 82 ohms |
| A19 | R7 | None | 200 ohms |
| A20 | R2, R17 | Not used | Removed |
| | CR19, CR20 | None | 1N270 |

## 1-5. Uses and Capabilities

*a. General.* The vlf-12B, shown in figure 1-1, is a highly sensitive, ultra-stable instrument designed for phase-locked reception and tracking of vlf standard time and frequency transmissions. The major application of the vlf-12B is to provide data representing the cumulative frequency offset between a vlf frequency time transmission and a local frequency standard. The frequency offset is recorded in microseconds on a time difference register on a chart recorder located on the front panel. This information is used to calibrate the local frequency standard and to determine the crystal oscillator aging characteristics. Accuracies of 1 part in $10^9$ over approximately a 30-minute measurement interval and 2 parts in $10^{11}$ over a 24-hour observation interval are readily obtainable. Uses of the vlf-12B receiver-phase comparator include the following:

(1) Frequency measurement, calibration, and performance monitoring of precision crystal oscillators, atomic frequency standards, and other comparably stable frequency sources.

(2) Timing and synchronization of precision clock systems.

(3) Investigation of vlf propagation phenomena.

(4) Navigation through use of stabilized carrier techniques.

*b. Frequency Measurement, Calibration, and Standardization.*

(1) Use of the vlf-12B for frequency calibration of any frequency standard having an available 100-kc or 1-mc output is simple and direct. The relative frequency error between the local frequency standard and the received vlf carrier signal may be observed on the time difference register (MICROSECONDS counter). Rate a time difference can be directly interpreted as a fractional frequency error in the local standard; thus, a phase rate of 1 $\mu$sec in a 100-second time interval represents a fractional frequency deviation of 1 part in $10^8$.

(2) To appreciate the magnitude of the time ratios involved, consider that:

1 min = 60 sec = $10^7$ $\mu$sec
1 hr = 3600 sec = $3.6 \times 10^9$ $\mu$sec
1 day = $8.64 \times 10^4$ sec = $8.64 \times 10^{10}$ $\mu$sec

and

1 $\mu$sec/min = $1.667 \times 10^{-8}$
1 $\mu$sec/hr = $2.78 \times 10^{-10}$
1 $\mu$sec/day = $1.16 \times 10^{-11}$

Corresponding frequency errors are expressed:

$$\text{Fractional frequency error} = \frac{\Delta f}{f} = \frac{\text{Difference in } \mu\text{sec}}{\text{Elapsed time in sec}} \times 10^{-6}$$

(3) Calculation can be made using the time-difference information taken from the chart recorder. Full-scale deflection of the chart trace represents a 100-$\mu$sec phase change, either positive or negative as the case may be, and frequency comparisons to an accuracy of parts in $10^9$ relative to the received vlf carrier can be obtained within an interval of 10 to 30 minutes.

(4) In reading the chart records of the accumulated phase error, it must be recognized that the recorder displays a maximum incremental range of 100 μsec. The total change in phase over an elapsed time interval can be obtained, however, by keeping a record of the full excursions of the recorder and by comparsion with the digital time-difference register. A discontinuity in the record occurs at the flyback point on the continuous-rotation recording potentiometer, but no data is lost because the trace will continue from the opposite edge of the chart. Frequency drift or aging characteristics of the oscillator can best be visualized by converting the basic data to a daily "frequency error" plot.

(5) Proper use of the vlf-12B record makes it possible to determine the performance of a local precision oscillator between calibration periods. After an initial run-in period, a crystal oscillator has a relatively constant aging rate. That is, its frequency becomes, for example, higher each day at a uniform rate. During the run-in period the aging rate is changing rapidly, but can be projected for several days.

(6) The run-in period consists of one to four months of continuous operation. Once placed in operation the oscillator should never be turned off; the entire run-in period must be repeated each time the oscillator is restarted.

(7) In using the vlf-12B with its chart recorder, it is important to know that the pen indicates change in phase; the movement of the chart indicates this change in phase as a function of time. Change in phase per unit time is frequency, so the slope of the pen line is frequency (rate) error. Change in the slope is change in rate error. These errors can be determined by continuous monitoring or by short monitoring periods at regular intervals.

(8) Precision of measurement is a function of observation noise, which is related to chart trace width and the period of observation or the period between observations, if the local oscillator is predictable between periods. For periods of one day, a typical high-quality crystal oscillator can be assumed to be predictable. An example of measurement and adjustment procedure is given below.

(9) Assume that observations are made once a day. On the first day ($t^0$) the local frequency standard was not adjusted. The second day ($t^1$) there is an indicated time error on the chart recorder and time-difference register of +50 μsec. If the elapsed time between observations was $10^5$ seconds (slightly over one day), the error in the frequency standard from nominal ($f_0$) was:

$$f_e = f_0 \times \frac{50 \times 10^{-6} \text{ sec error}}{10^5 \text{ sec elapsed time}} = f_0 \times 5 \times 10^{-10}$$

The frequency for that 24-hour period was $f = f_0 + f_e$, assuming no appreciable aging error.

(10) Ordinarily, the local frequency standard will have an adjustment knob with dial markings in increments of 1 pp $10^{-10}$. Adjust the knob 5 divisions to correct the frequency. The next day's observation indicates the accuracy of this adjustment by the resulting slope of the line.

(11) After the run-in period, the time gained each day will be virtually constant, and, if necessary, the frequency standard may be adjusted with considerable confidence without making a new observation, or the period between observations can be increased.

(12) In some applications it may be desirable that the oscillator be slightly overcompensated rather than set exactly on frequency whenever an adjustment is made. Thus, if experience indicates that the oscillator tends to drift (age) toward a higher frequency, the oscillator may be adjusted so that it starts off with a negative frequency deviation error. The overcompensation technique will result in the maximum time interval before another adjustment will be required to maintain the oscillator within specified tolerances.

(13) Selection of the vlf station to be used for frequency correlation purposes depends upon many factors. Groups involved in global network operation will undoubtedly be instructed to monitor some particular transmitter that can be reliably tracked at all receiving sites. Selection of one or more secondary stations is advisable so that no receiving

site is wholly dependent upon a single transmitter. The stations are listed in paragraph 1-7.

*c. Clock Synchronization.* It is possible to use the vlf transmissions directly for time-of-day information purposes. Station NBA, for example, transmits timing pulses at precise 1-second intervals. Unfortunately, the modulation envelope of the keyed carrier has such a slow rise time that the beginning of the transmitted time pulse is difficult to recognize. The NBA transmitted signal has a rise time in the neighborhood of 15 milliseconds because of a transmitting antenna Q of roughly 700. This is required to achieve reasonable radiating efficiency at the low frequency. Nevertheless, various schemes to obtain reliable synchronization points on the leading slope of the modulation have been developed, and are being used successfully to achieve clock settings.

*d. Investigation of VLF Propagation Phenomena.*

(1) Investigations of vlf propagation phenomena are being carried out by various agencies, here and abroad. These include studies of the diurnal change of altitude in the vlf-reflecting D layer of the atmosphere; studies of the effects of magnetic and sudden ionospheric disturbances; and comparisons of reception of the various vlf transmissions.

(2) The ultra stability of vlf transmissions is true for cases where the entire propagation path is either in daylight or in darkness, with daytime transmissions being the more stable. During periods of sunrise or sunset there is a shift in phase of about 200° (36 $\mu$sec at 18 kc). The period of the shift is determined by the difference in longitude between the transmitter and the receiver, and by the seasonal variations in the length of twilight; if there is a difference of 75° in longitude, the shift will occur over approximately 5 hours. These diurnal shifts (sunrise and sunset) are equal in magnitude and opposite in direction, and extremely regular. The only real changes are due to the ordinary seasonal variation in the length of the day and night and the duration of twilight. With a little local experience, the diurnal shifts can be predicted and frequency calibration can be accomplished even during the shifts (of course, the shifts cancel for a 24-hour observation period).

(3) Magnetic storms produce a turbulent effect on nighttime transmission, but daytime transmission is virtually unaffected. Sudden ionospheric disturbances (S.I.D.) can produce phase shifts as large as 100° in 5 minutes, with recovery taking about an hour. The S.I.D. effects cannot be predicted, of course, but can be identified by the sharp rise and slow recovery, and can then either be discounted or removed analytically from the frequency comparison.

(4) A typical vlf-12B chart record illustration of diurnal shift and sudden ionospheric disturbance is shown in figure 1-2. The sunrise and sunset effects are shown for a transmitter about 30° longitude west of the receiver. An S.I.D. is shown occurring at 10 o'clock.

*e. Navigation.* VLF transmissions can be used for navigation purposes in areas where LORAN C or OMEGA transmissions are not received. For this application a precision frequency standard, two vlf-12B's, a dual-channel chart recorder, and some form of compensation for radial velocity with respect to the vlf stations are required. It has been reported that dead-reckoning navigational accuracy of 1 mile or less can be realized during all daylight conditions.

## 1-6. VLF Time Service Stations

*a.* VLF stations which transmit on a basis of controlled carrier frequencies are listed in table 1-3.

*Table 1-3. VLF Time Service Stations*

| Station | Frequency (kc) | Location | Sponsor |
|---|---|---|---|
| OMEGA | 10.2 | Various; Global Net | U.S. Navy |
| GBR | 16.0 | Rugby, England | RNOUK |
| FUB | 16.8 | Paris, France | |

*Table 1-3. VLF Time Service Stations*—Continued

| Station | Frequency (kc) | Location | Sponsor |
|---|---|---|---|
| NAA | 17.8 | Cutler, Maine | U.S. Navy |
| NPG/NKL | 18.6 | Jim Creek, Washington | U.S. Navy |
| GQD | 19.0 | Anthorn, Scotland | NATO |
| GBZ | 19.6 | Liverpool, U. K. | KNOUK |
| WWVL | 20.0 | Ft. Collins, Colorado | National Bureau of Standards |
| NSS | 21.4 | Annapolis, Maryland | U.S. Navy |
| NBA | 24.0 | Balboa, Canal Zone | U.S. Navy |
| NPM | 26.1 | Lauluale i, Hawaii | U.S. Navy |
| WWVB | 60.0 | Boulder, Colorado | National Bureau of Standards |

*b.* The U.S. Navy frequency assignments are subject to change without notice. The frequencies listed are those in use as of January 1965. All stations except WWVB operate on UT2 Time Base; WWVB uses A.1 Time Base.

*c.* The Time Service Stations of the U.S. and the United Kingdom are coordinated in time and frequency by vlf links. All the stations in the coordination plan have transmitters stabilized by Atomicron (cesium) clocks. Time pulses are synchronized with the stabilized carrier frequency, which is offset from A.1 to minimize the difference between A.1 and UT2. The frequency transmitted remains constant throughout any one year, and is specified as follows: $F = F_o (1 + 5)$, where $F_o$ is the nominal frequency of the transmitter and s is the fractional offset which gives a rate most nearly equal to the rate of UT2. The fractional offset for any year is jointly determined, in advance, by the Royal Greenwich Observatory and the U.S. Naval Observatory. The value for both 1964 and 1965 was $-150 \times 10^{-10}$.

*d.* The value of the fractional offset is broadcast each 15 minutes in International Morse Code, so A.1 can readily be determined from the received carrier frequency.

*e.* Seconds pulses are locked in phase with the carrier frequency. Whenever the seconds pulses depart too far from UT2, the clocks at all the transmitting stations are shifted 50 milliseconds on the first of a month. The changes are jointly determined by the Royal Greenwich Observatory and the U. S. Naval Observatory. No more than one or two such changes will ever be necessary in one year.

*f.* U. S. Naval Observatory Time Signal Bulletins A and B give final corrections to transmitted frequencies to obtain UT2, UT1, and UT0 and A.1. The differences between Apparent and Mean Solar and Sidereal Times (the "equation of time" and the "equation of the equinoxes", respectively) are tabulated in the American Ephemeris and Nautical Almanac.

## 1-7. Technical Characteristics

Table 1-4 lists the technical characteristics for the vlf-12B.

*Table 1-4. Technical Characteristics*

| Feature | Characteristics |
|---|---|
| Frequency Coverage | VLF channel tracking is provided in 100-cps increments for all possible channels in the frequency spectrum between 10 kc and 30 kc. Channel selection is entirely by thumbwheel switches with position detent. Channel selection is positive and accurate without the use of plug-in filters and without further adjustment of the local oscillator, rf selectivity, or any other frequency-determining circuits.<br>A 60-kc channel, selectable by means of a separate front-panel switch, is also provided. No tuning is required for optimum operation. |

*Table 1-4. Technical Characteristics*—Continued

| Feature | Characteristics |
|---|---|
| Bandwidths | Bandwidth restriction is supplied at appropriate locations within the receiver to ensure the desired signal-handling capability of each function described:<br>RF module pass band (single filter) for 60-db image rejection: 8 to 30 kc<br>First intermediate frequency (12.25 kc) pass band: 200 cps<br>Second intermediate frequency (1 kc) pass band: 50 cps (nominal)<br>Phase-tracking servo bandwidth: 0.006 cps (nominal) |
| Receiver Sensitivity | An input level of 0.01 microvolt across 50 ohms and a signal-to-noise ratio of –50 db (Gaussian noise measured in a 1-kc bandwidth) will result in accurate phase tracking with a nominal servo bandwidth of 0.006 cps.<br>The noise figure of the receiver is less than 20 db, and internal receiver noise will not cause the chart recorder or the time difference register to display more than 0.3 microsecond jitter. The limit on jitter, caused by internal receiver noise, exists when the receiver is tracking a 0.01-microvolt signal from a coherent generator and the nominal servo bandwidth is 0.006 cps. |
| Signal Level Operating Range | The total operating range of signal level is 120 db. This range is accomplished by the use of a manual step attenuator having a range of 80 db in 10-db steps coupled with a minimum of 40 db of automatic gain control (agc). |
| Automatic Gain Control (AGC) | A stable agc circuit assures reliable phase tracking over a 40-db range of input carrier level with less than 0.5 microsecond of phase shift. The detection of the agc signal is accomplished by the use of a quadrature detector designed to provide agc, regardless of phase between the received station and the local standard. |
| Response to Undersirable Signals | The following characteristics are given assuming a normal input level of 1 microvolt for the desired signal, and assuming that all receiver controls are optimized: |
| Adjacent Channel Rejection | A coherent signal 100 cps from the desired signal and 30 db larger in amplitude will not adversely affect the phase tracking of the desired signal. Similarly, a signal 200 cps or more from the desired signal and 60 db larger in amplitude will not affect the phase tracking of the desired signal. |
| Spurious Responses | The spectral purity of the mixing frequencies within the vlf-12B are sufficient to provide any undesired responses, 100 cps or more from the channel selected by the thumbwheel switches, from limiting the adjacent channel rejection characteristics specified. |
| Image Rejection | Image rejection is 60 db or greater at all selected frequencies without the use of plug-in filters and without repositioning the local oscillator. |
| Desensitization | With the receiver properly tuned to a desired channel, and undesired signal located 200 cps or more in frequency from the desired channel, and 60 db larger in amplitude, will not lower the gain of the receiver to the desired signal by more than 3 db. |

*Table 1-4. Technical Characteristics*—Continued

| Feature | Characteristics |
|---|---|
| Intermodulation and Harmonic Distortion Response | All second- and third-order products of the desired and undesired channels are 60 db lower in amplitude than the input signal. |
| Frequency Synthesizer | The choice of the first intermediate frequency and the design of the frequency synthesizer produce a local-oscillator injection frequency that is locked in 100-cps increments but offset by 50 cps from the normal 100-cps increment; e.g., 24.25 kc, 24.35 kc, 24.45 kc. The frequency offset prevents any local-oscillator signals radiated by the antenna from interfering with other coherent phase detector, since the discrete frequencies are not phase-coherent to the normal vlf channel frequencies. The frequency-selecting switches set the desired 100-cps increment and provide direct indication of the desired vlf station frequency. After being switched to another frequency and then returned to an original setting, the synthesizer phase shift is less than 0.5 microsecond. |
| Coherent Signal Radiation | The phase-coherent signal level present at the 50-ohm antenna input connector is less than –167 dbm (0.001 microvolt). |
| Receiver Inputs | Two separate rf inputs, 50 ohms and 10K nominal, are supplied with BNC connectors mounted on the rear panel.<br>A 100–kc frequency standard input is provided by means of a BNC connector on the rear panel. The nominal 10K input accommodates a signal level between 0.5 volt and 15 volts rms. |
| Receiver Outputs | The following outputs are available on the rear panel BNC connectors:<br>Amplified vlf carrier at a 1-kc intermediate frequency and 200-cps bandwidth that carries the same phase information as the received signal.<br>100-kc square wave that is coherent with the vlf carrier and is a nominal 1 volt pp across 50 ohms.<br>10-kc square wave that is coherent with the vlf carrier and is a nominal 1 volt pp across 50 ohms.<br>1-kc square wave that is coherent with the vlf carrier and is a nominal 1 volt pp across 50 ohms.<br>100-cps square wave that is coherent with the vlf carrier and is a nominal 1 volt pp across 50 ohms.<br>DC output voltage that is accurately proportional to the relative phase difference between the local standard and the vlf carrier, for driving a nominal 1-ma external recorder or the internal recorder. A rear chassis potentiometer adjustment provides span calibration to obtain a full-scale chart deflection that represents 100 microseconds of phase change. A rear panel switch is provided to connect the phase difference output voltage to either the external or internal recorder.<br>The following outputs are available on the front panel:<br>A built-in chart recorder with inkless stylus and a chart speed of 1 inch per hour. Full-scale calibration of the chart paper is 100 microseconds.<br>Built-in speaker for aural monitoring of the 1-kc if. A front-panel volume control provides adequate range to shut off the audio signal completely |

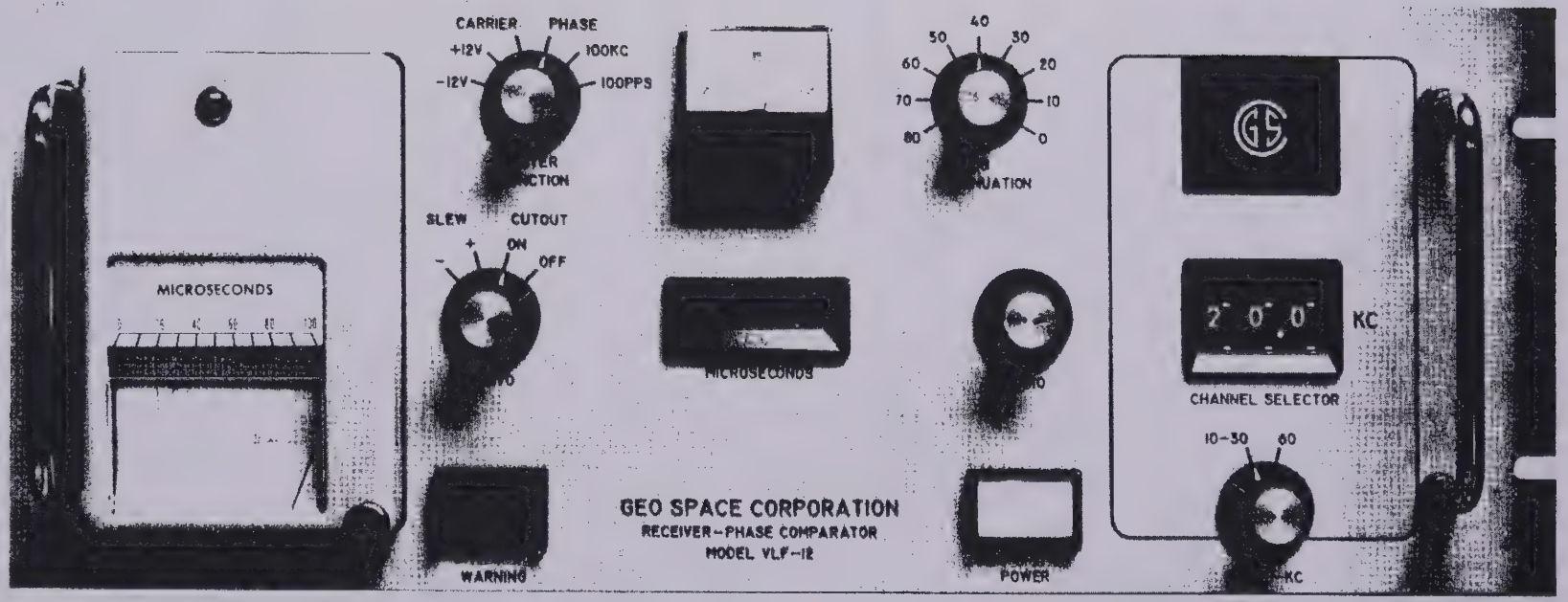
*Table 1-4. Technical Characteristics*—Continued

| Feature | Characteristics |
|---|---|
| | or to provide sufficient audio power for use in conventional operating environments. |
| Phase-Tracking Servo | An electromechanical servo maintains a phase-shifted reference signal in a phase-null condition relative to a selected vlf carrier.<br>Servo deadband is ± 0.1 μsec, nominal.<br>Phase-tracking error is less than 5 μsec at the maximum fractional frequency offset (1 pp $10^7$).<br>Manual servo slewing switch, located on the front panel, advances or retards the phase-tracking servo at approximately twice the rate experienced at the maximum fractional frequency offset or for a given receiver time constant. |
| Meter Display | A front-panel meter, with special calibrated dial markings, monitors signals that the operator must observe to determine the performance status of the receiver. The signal or level is selected by the METER FUNCTION switch to allow individual and independent monitoring of the following signals:<br>Relative carrier level<br>Phase detector error voltage<br>Positive supply voltage<br>Negative supply voltage<br>Indication of proper operation of 100-kc frequency standard input<br>Indication of proper operation of 100-cps synthesizer signal |
| Interrupt Warning | The front-panel indicator provides a warning if interruption in the ac power or the local frequency-standard input has occurred. Only the indication is manually resettable; the vlf-12B returns automatically to normal operation when service is restored. Another front-panel indicator warns of any loss of carrier, and will automatically turn off when the carrier is returned. |
| Time Difference Register | A front-panel digital MICROSECONDS counter, driven by the servo, displays the relative time difference between the local standard and the vlf carrier. The counter is cumulative to 9999.9 microseconds. |
| Calibration Accuracy | The calibration accuracy, relative to a received carrier, is better than ± 1 x $10^{11}$ on a 24-hour basis, over the specified temperature range and input ac line-voltage variation tolerance. |
| Environment | The vlf-12B operates properly over a range of –20° C to +65° C at a relative humidity of 95%. Total receiver phase shift from all causes is less than ± 1.0 μsec over a temperature range of 0° C to 50° C. The receiver is designed to withstand the shock and vibration encountered during normal shipping. |
| Power Requirements | The vlf-12B operates from an ac power source of 95 to 130 volts rms, 48 to 600 cps, at a power level of less than 25 watts. All of the basic specifications are maintained over these ac line-voltage variations. If a recorder is supplied, the synchronous motor must be chosen to suit the line frequency. The vlf-12B may also be connected to a 24-volt dc standby source to enable automatic operation in the event the ac power should fail. |

## 1-8. Physical Description

*a.* The vlf-12B is designed to be mounted in a standard 19-inch rack position not more than 7 inches high, and requires no more than 18 inches in depth behind the front panel. The net weight is approximately 45 pounds.

*b.* The unit is constructed of functional modules arranged for ease of maintenance and troubleshooting. Each module has adequate test points to isolate any trouble within a particular module. All points are accessible for monitoring without interrupting normal operation. An extender card is provided for incircuit testing, and a card extractor is provided to allow easy removal of printed-circuit cards.




EL5895—413—15/3—1

*Figure 1–1. VLF–12B receiver-phase comparator*



TM 11-5895-413-15/3/NAVSHIPS 0967-301-5230/TO 3155-2FYQ42-161

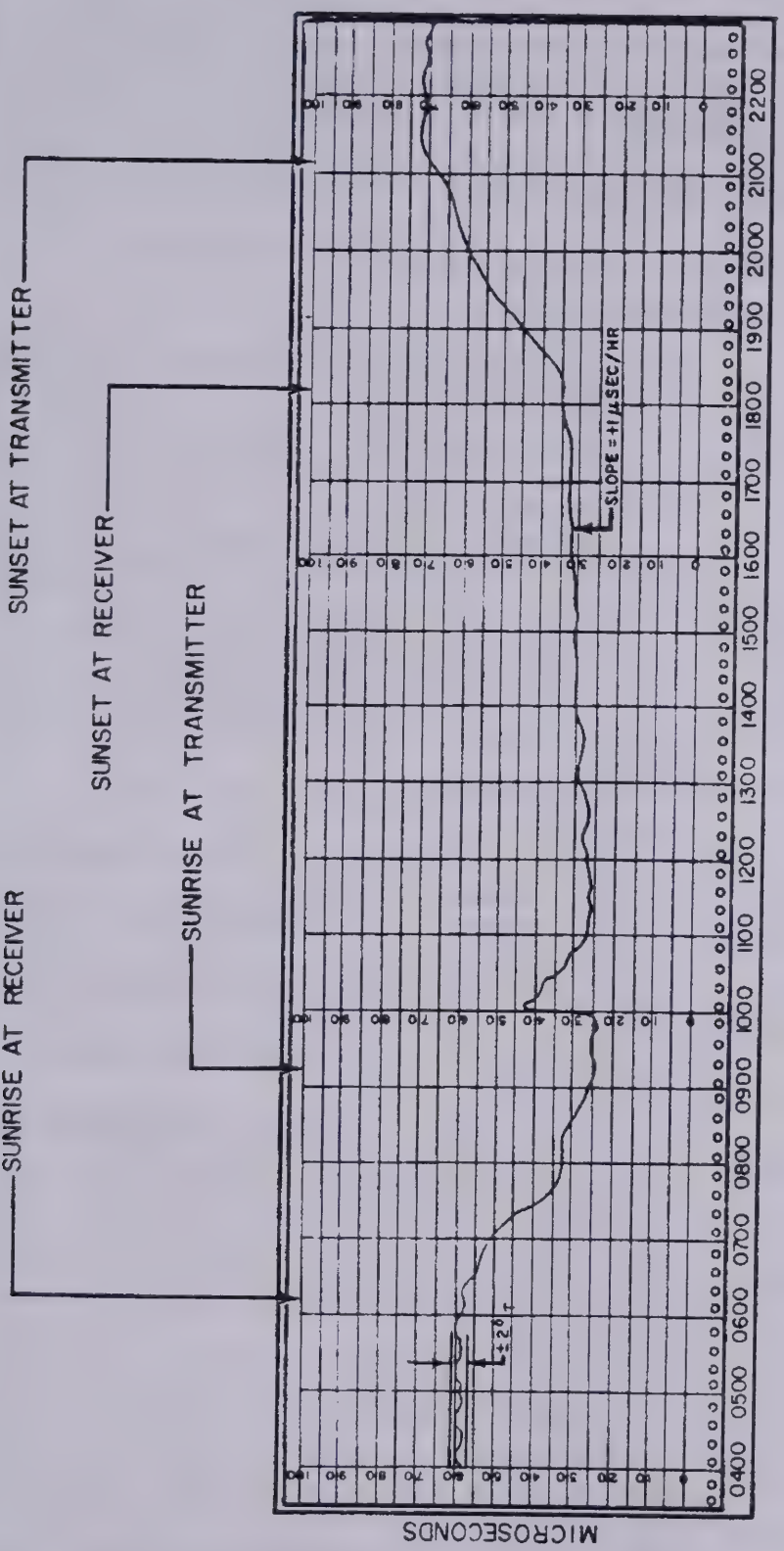

SUNRISE AT RECEIVER
SUNSET AT TRANSMITTER
SUNRISE AT TRANSMITTER
SUNSET AT RECEIVER
SLOPE = +11 μSEC/HR
± 2σ τ
MICROSECONDS
LOCAL TIME
0400 0500 0600 0700 0800 0900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200
EL5895-413-15/3-2

*Figure 1-2. Typical vlf-12B receiver-phase comparator chart record, illustrating diurnal shift*

# CHAPTER 2

# INSTALLATION AND OPERATION

## Section I. INSTALLATION

### 2–1. General

This section contains detailed instructions for unpacking and installing the vlf-12B receiver-phase comparator.

### 2–2. Unpacking and Checking the Equipment

When packed for export shipment, the vlf-12B is contained in a typical package as shown in figure 2–1. To avoid damage to equipment during unpacking, carefully follow the steps below:

*a.* Transport package to desired operating location.

*b.* Cut and fold back metal straps.

*c.* Remove nails from top and one side of wooden box with nail puller. Do not attempt to pry lids.

*d.* Open moisture-proof barrier that covers the carton inside the wooden box, and remove carton.

*e.* Open carton and second moisture-vapor-proof barrier within the carton.

*f.* Remove inner carton. Open inner carton and remove equipment.

*Caution:* **Never use sharp tools or instruments when opening cartons, as they may cause damage to the equipment.**

*g.* Upon removal of equipment from the containers, check to see whether all items shipped agree with packing list. Inspect exterior for any visible signs of damage, such as dents, nicks, or scratches, and broken or loose control knobs. Report any defects immediately.

### 2–3. Tools and Equipment Required for Installation

*a.* For vlf-12B's supplied with a cabinet intended for bench mounting, no installation is required and therefore no tools are required.

*b.* VLF-12B's intended for installation in a standard 19-inch equipment rack can be accommodated in a space adequate for the 7-inch panel height. The depth of the rack should be at least 22 inches to allow for connector clearance. Tools and hardware required to install the equipment in the rack include the following:

(1) Screwdrivers, common and Phillips head, 6 and 8 inch

(2) Set of small sockets (1/4-inch drive)

(3) 1/4-inch power drill

(4) Assortment of drill bits (for metal), 1/16 to 1/4 inch in 32nds

(5) Countersink bit (depending upon rack used)

(6) Nuts, bolts, and assorted flat and split lockwashers

*c.* Ancillary equipment required includes: a long-wire, whip, or loop antenna; a power cord (normally supplied with receiver); and two 50-ohm coaxial cables of appropriate length with BNC connectors to connect the antenna and local frequency standard to the receiver. A list of mating connectors is given in table 2–1.

### 2–4. Installation Procedure

*a.* If the vlf-12B is cabinet mounted, it is necessary only to connect the power cord, the antenna lead-in, and the coaxial line from the local standard to the designated connectors

at the rear of the chassis. If a long-wire antenna is used, connect to the HI Z input. If a whip or loop antenna is used, connect to the 50Ω input. It is not necessary to use 50-ohm coaxial lead-in with the long-wire antenna, but use of a shielded line, of some type, to minimize strong local interference is recommended.

*b.* For installation of a vlf-12B equipped with drawer slides, consult the equipment mounting instructions supplied with the particular rack used. With most commonly available racks, it is necessary only to bolt the slides to predrilled rack bars. With some racks it is necessary to drill special holes to accommodate the slides.

*Table 2-1. List of Mating Connectors*

| Function | Chassis connector | Mating connector |
|---|---|---|
| 50-ohm antenna | BNC type UG-1094/U | Note 1 |
| Hi Z antenna | BNC type UG-1094/U | Note 1 |
| 100-kc coherent | BNC type UG-1094/U | Note 1 |
| 10-kc coherent | BNC type UG-1094/U | Note 1 |
| 1-kc coherent | BNC type UG-1094/U | Note 1 |
| 0.1-kc coherent | BNC type UG-1094/U | Note 1 |
| Local standard input | BNC type UG-1094/U | Note 1 |
| 1-kc if. | BNC type UG-1094/U | Note 1 |
| External recorder | BNC type UG-1094/U | Note 1 |
| AC power | Note 2 | MS 3106A 10SL-35 (C) |

Note 1: With RG-174/U cable use Gremar type 6399.
With RG-58/U cable use BNC type UG-88/U.
With RG-62/U cable use BNC type-260/U.
Note 2: Chassis connector is integral part of rfi filter.

## Section II. OPERATION

### 2-5. General

This section provides information on all operating controls, indicators, and connectors, plus instructions for operating the vlf-12B. Refer to figures 2-2 and 2-3 for locations, and to table 2-2 for functions of the controls, indicators, and connectors.

### 2-6. Preoperational Procedure

When the vlf-12B is to be put into actual service, the following instructions should be carried out step by step.

*a.* Connect the three-conductor line cord to the AC POWER connector provided on the rear panel.

*b.* Plug the cord into an outlet providing a nominal 120 volts ac at any line frequency from 48 to 600 cps. If standby dc power is to be used, connect the +24 volt dc source to the D.C. POWER connector on the rear panel.

*c.* Connect an available antenna to the appropriate input, 50Ω or HI Z, depending upon the impedance of the antenna circuit (long wire—HI Z; loop or whip—50Ω).

*d.* Connect either the 100-kc or 76.8-kc signal (0.5 to 15 volts, rms) from a local standard frequency source to the LOCAL STD connector on the rear panel. Set the 76.8 kc/100 kc selector switch, which is adjacent and to the right of the connector, to the appropriate local reference frequency.

*e.* Loosen the knurled thumbscrew and open the recorder panel to discharge the static on the chart paper; then set the record switch, located on the rear panel, to the INT. position. Position recorder stylus, with the mechanical screwdriver adjust, to the center of the scale. (The mechanical adjust is located under a snap button hole plug at the top center of the recorder panel.) Close panel and tighten the knurled thumbscrew.

*f.* Set AUDIO volume control at midrange.

*g.* Set DB ATTENUATION control to 80 db.

*Table 2–3. Controls, Indicators, and Connectors*

| Name | Ref des | Function |
|---|---|---|
| | | Front panel |
| METER FUNCTION Selector Switch | S7 | A rotary switch which permits selective monitoring of six frequently used test points when making pre-operational checks when maintaining the vlf–12B.<br>The functions monitored are:<br>–12V: Output voltage of –12-volt power supply.<br>+12V: Output voltage of +12-volt power supply.<br>CARRIER: The instantaneous relative strength of the carrier level. The total meter range is 50 db.<br>PHASE: The instantaneous relative phase shift of the reference frequency with respect to the coherent input, within a range of ± 0.5 radian.<br>100KC: The local standard 100-kc input. Proper operation is indicated by a midscale meter reading.<br>100PPS: The 100-pps corrected output. Indicates the correct operation of the entire output divider chain. Proper operation is indicated by a midscale meter reading. |
| Meter | M1 | Provides indications of power levels and signal performance as selected by the METER FUNCTION switch. |
| Chart Recorder | M2 | An integral chart recorder which provides a cumulative record of local reference frequency time shift with respect to the incoming standard signal. The recorder has an inkless stylus and a chart speed of 1 inch per hour. |
| SERVO Selector Switch | S8 | Permits operation of the servo in two basic modes, as follows:<br>Manual Slewing: Direction is determined by selecting either + or – SLEW.<br>Automatic Track: In the CUTOUT ON position, an automatic cutout is activated which will disconnect the servo if carrier fails or falls to a level too low for reliable tracking. The servo is automatically reconnected whenever carrier returns. In the CUTOUT OFF position, the servo is connected continuously. |
| INTERRUPT WARNING Lamp and Latching Relay | S9 | When either local standard input or ac power is interrupted, the upper half of the dual indicator pushbutton will display PWR/STD and remain lighted. Whenever the carrier strength falls below a level which is normally required for reliable phase tracking, the lower half will indicate loss of carrier and remain lighted. The PWR/STD indicator stores information related to continuity of signal and power inputs when left unattended and will do so until manually reset by depressing the indicator/pushbutton device. The CARRIER indicator remains lighted only during the actual absence of the vlf carrier and will extinguish without manual resetting when the carrier returns. |
| MICROSECONDS Time Difference Register | P/O A27 | A digital counter which provides cumulative time difference registration of the frequency standard phase shift up to 9999.9 microseconds. |
| DB ATTENUATION | A1S1 or H0A1 | Permits attenuation of the input signal of the RF section in 10-db intervals over a range of 0 to 80 db. |

*Table 2-3. Controls Indicators, and Connectors*—Connectors

| Name | Ref des | Function |
|---|---|---|
| | | **Front panel** |
| POWER ON Switch | S5 | A pushbutton switch that turns ac power on and off for the entire vlf-12B. When power is on, the switch is illuminated. |
| Loudspeaker | LS1 | Provides an aural indication of the vlf carrier modulation. |
| CHANNEL SELECTOR Switch | S1, S2, S3 | Permits frequency selection, which is accomplished by positioning the three thumbwheel switches to settings that correspond numerically to the desired input frequency. The entire 10- to 30-kc vlf band, in steps of 0.1 kc, is covered with this selector. |
| AUDIO Level Control | | Permits control of the audio modulation volume. |
| RANGE-KC | S4 | Enables selection of the 10 to 30-kc band or the 60-kc channel. |
| | | **Rear panel** |
| ANTENNA | J1<br>J2 | The 50Ω input connector (J1) is intended for use with whip and loop antennas. The HI-Z input connector (J2) is intended for use with long-wire antennas. |
| COHERENT Outputs | J7(.1KC)<br>J6(1KC)<br>J5(10KC)<br>J4(100KC) | Four coherent signal buffered outputs are provided for external use. The receptacles labeled 100 KC, 10 KC, 1 KC, and 0.1 KC furnish square waves at a nominal 1 volt peak-to-peak. All are phase-locked to the vlf carrier. |
| LOCAL STD Input | J3 | Provides for the connection of either a 76.8-kc or a 100-kc local frequency standard. Appropriate positioning of the adjacent toggle switch adapts the vlf-12B to the chosen local standard. |
| 1KC IF Output | J8 | A receptacle that provides buffered access to the 2nd if. signal which is coherent with the vlf carrier. It may be used for external monitoring. |
| RECORDER | R2<br>(Potentiometer)<br>S/O<br>(toggle Sw)<br>J9<br>(Connector) | Calibration adjustment for FS ADJ (R2) is for full-scale adjustment of the internal strip chart recorder. The INT. and EXT. selector switch (S10) permits use of either the internal or an external chart recorder attached to the EXT. connector (J9). This provision enables simultaneous monitoring of the cumulative reference frequency shift time and amplitude indication signals. |
| D.C. POWER Input | J11 | Terminals provided on the rear panel for the connection of a +24 volt dc standby source. Transfer to the stand-by power source is accomplished automatically, without interruption or loss of phase tracking, if ac power should fail. |
| AC POWER Input | J10 | A 3-pin connector which accepts the 120-volt ac primary power to the vlf-12B. |
| Fuse | F1 | 1/2-ampere slo-blo fuse in series with the primary ac power input. |

*h.* Set SERVO selector switch to CUTOUT ON position.

*i.* Set RANGE-KC selector switch to 10–30 KC position.

*j.* Set the digital thumbwheel CHANNEL SELECTOR switch on the front panel to the desired vlf station frequency.

*k.* Depress the indicator/pushbutton POWER switch to apply primary power to the vlf-12B.

*l.* Set the METER FUNCTION selector switch successively to each of the six monitoring positions. Normal conditions are indicated as follows:

| *Meter Function* | *Meter Indication* |
|---|---|
| -12V | Red mark on right of center |
| +12V | Red mark on right of center |
| CARRIER | In green area when proper attenuator position is selected. |
| PHASE | In green area when phase-locked. |
| 100KC | In green area |
| 100PPS | In green area |

*m.* Adjust DB ATTENUATION control, if necessary, to bring meter indication of carrier level into green area. Slowly step DB ATTENUATION switch downward, allowing sufficient time for agc time constant to charge between steps, until the front panel meter reads approximately center scale. If the relative signal strength is known for the particular transmitting station and the geographical location and antenna characteristics of the receiving station, DB ATTENUATION switch can be preset to the desired position.

*n.* Set AUDIO volume control to desired volume for continuous monitoring.

*o.* Make a quick check of proper servo operation by setting selector switch to -SLEW or +SLEW. When set at -SLEW, the servo will slew in a negative direction, and an indication of negative change can be observed at the time difference register. In the +SLEW position an opposite indication will be obtained. When the slew check is completed, the SERVO selector switch should be returned to an automatic tracking position. This procedure will enable the operator to determine whether the servo is tracking the vlf transmission. When the switch is returned to CUTOUT ON, the time difference register should indicate the original reading or number which closely approaches the value. The normal position for the selector switch is CUTOUT ON. In this position the servo will be automatically disconnected if the carrier level falls below the level required for reliable tracking, and will be reconnected when the carrier returns to the proper level. The servo can be made to remain in operation by positioning the selector to CUTOUT OFF. In this position the servo is activated at all times and will allow tracking of weak signals which are below the threshold level of the cutout circuit.

## 2-7. Utilizing VLF-12B for Frequency Source Comparison and Adjustment

*a.* Various applications for the vlf-12B have been explained in previous paragraphs. The most often used, however, is that of rating and adjusting precision frequency source equipment by determining the rate of time error drift of the local frequency standard with respect to a vlf standard time and frequency broadcast.

*b.* After preliminary checks and adjustments have been made and it has been determined that the vlf-12B is tracking properly, comparison measurements may be made and frequency standard corrections may be derived by recording and interpreting data as follows:

(1) Set up a chart of time difference register readings versus time, date, and hour for the interval recommended by the frequency standard manufacturer.

(2) Take an initial reading of the time difference register, and record and plot the reading versus time. The numerical value of the reading is of importance only as a reference to which all subsequent readings are compared. If preferred, the dial can be manually set to zero at the beginning of the sequence, but once the reference is established, the time difference register must not be readjusted until the entire procedure is completed. The relative frequency error between the local frequency standard and the vlf signal is observed as an integral time difference in microseconds. A maximum cumulative error of 9999.9 microseconds is possible.

(3) Mark the date and time of initial reading near the stylus on the vlf-12B chart recorder.

(4) Make a second reading of the time difference register after the previously scheduled interval has passed. Record and plot the results as before, and make sure that the time of the reading is also recorded of the chart record. An initial rate of drift error can be calculated by use of the following relationship:

$$\frac{\triangle f}{f} = \text{Fractional frequency error} = \frac{\text{Difference in } \mu \text{ sec}}{\text{Elapsed time in sec}} \times 10^{-6}$$

Assume that the register reading at 8:00 a.m. on a particular day is 4376.5 and at 2:15 p.m. of the same day the reading is 4323.2. The net difference in microseconds over the 6 hour and 15 minute (22,500 seconds) interval is 4376.5–4323.2, or –53.3 microseconds. Therefore the fractional frequency error is:

$$\frac{-53.3}{22{,}500} \times 10^{-6} = -2.37 \times 10^{-9}$$

The minus sign indicates that the reading at the 6.25-hour interval was lower than the initial reading and implies that the local standard frequency is low. Conversely, an increase in the reading would imply that the local standard frequency is high with respect to the comparison frequency derived from the selected vlf carrier. Similar results can be obtained from the chart recorder. It must be realized, however, that each off-scale reading of the chart recorder represents a 100-microsecond change. The direction of the off-scale readings is important, since one direction indicates an increase and the other a decrease in frequency error. Unlike the time difference register, the chart recorder provides a permanent record of all variations in the relative frequency or phase difference between the sources being compared, as well as indications of frequency drift trends and of diurnal changes along the vlf propagation path. It should be referred to when rate of drift is computed from time difference register readings.

(5) The information obtained from the steps above can be used directly to make initial adjustments on the frequency standard or to determine aging characteristics of crystal standards. See instructions accompanying the oscillator standard for complete adjustment procedure.

## 2–8. Stopping Procedure

Although no damage can be done by not following a predetermined shutdown procedure, it is helpful to preset the controls to be ready for the next operation. The following procedure can be used.

*a.* Set DB ATTENUATION control to 80 db.

*b.* Set SERVO selector switch to CUTOUT ON.

*c.* Set AUDIO volume control at midrange.

*d.* Depress POWER switch to shut off primary power.

*Note.* If the vlf-12B is supplied with an external dc battery pack, the dc power should be disconnected when the equipment is shut down to prevent battery drain during periods of inactivity.

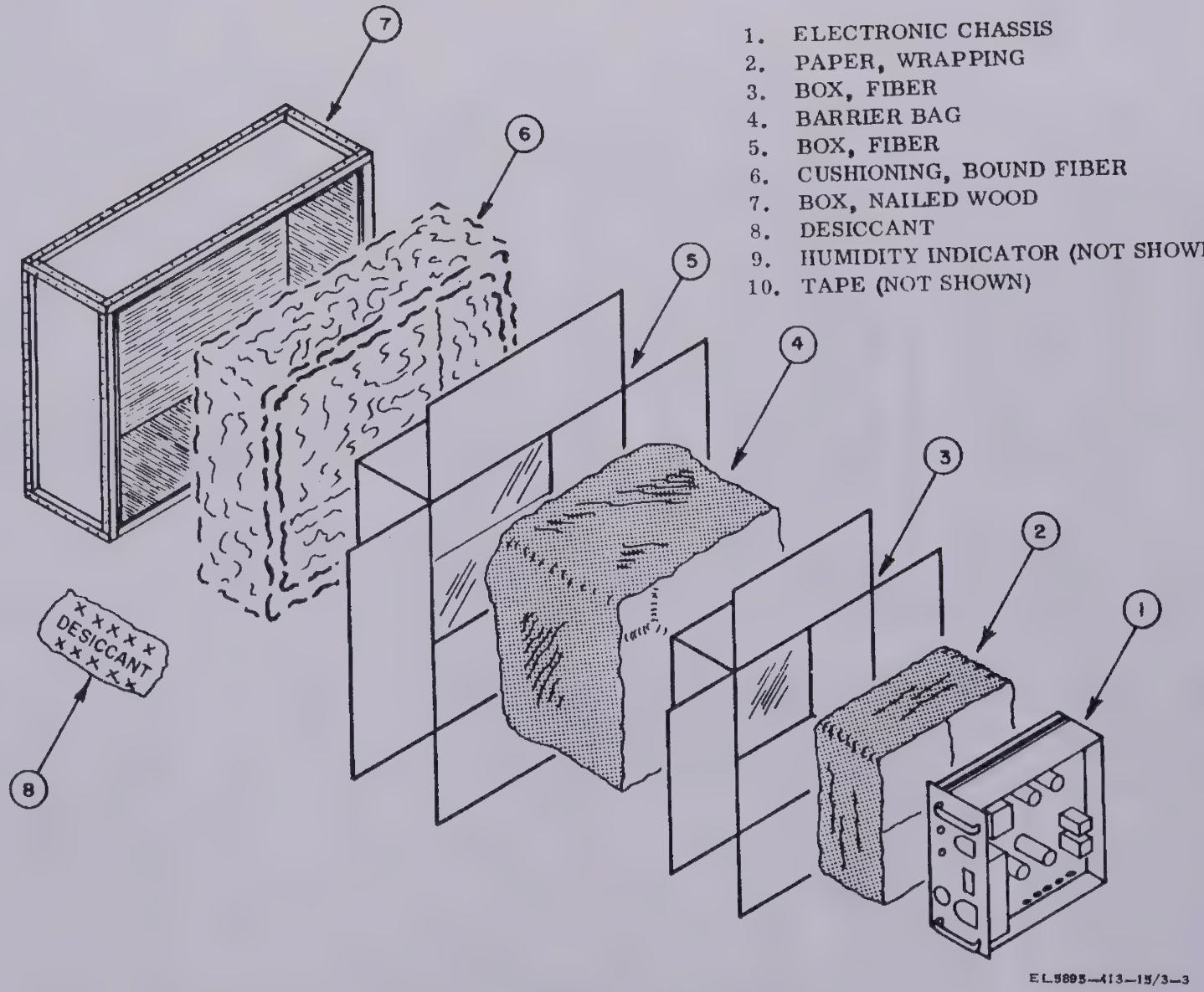



*Figure 2-1. Typical packing for export shipment*

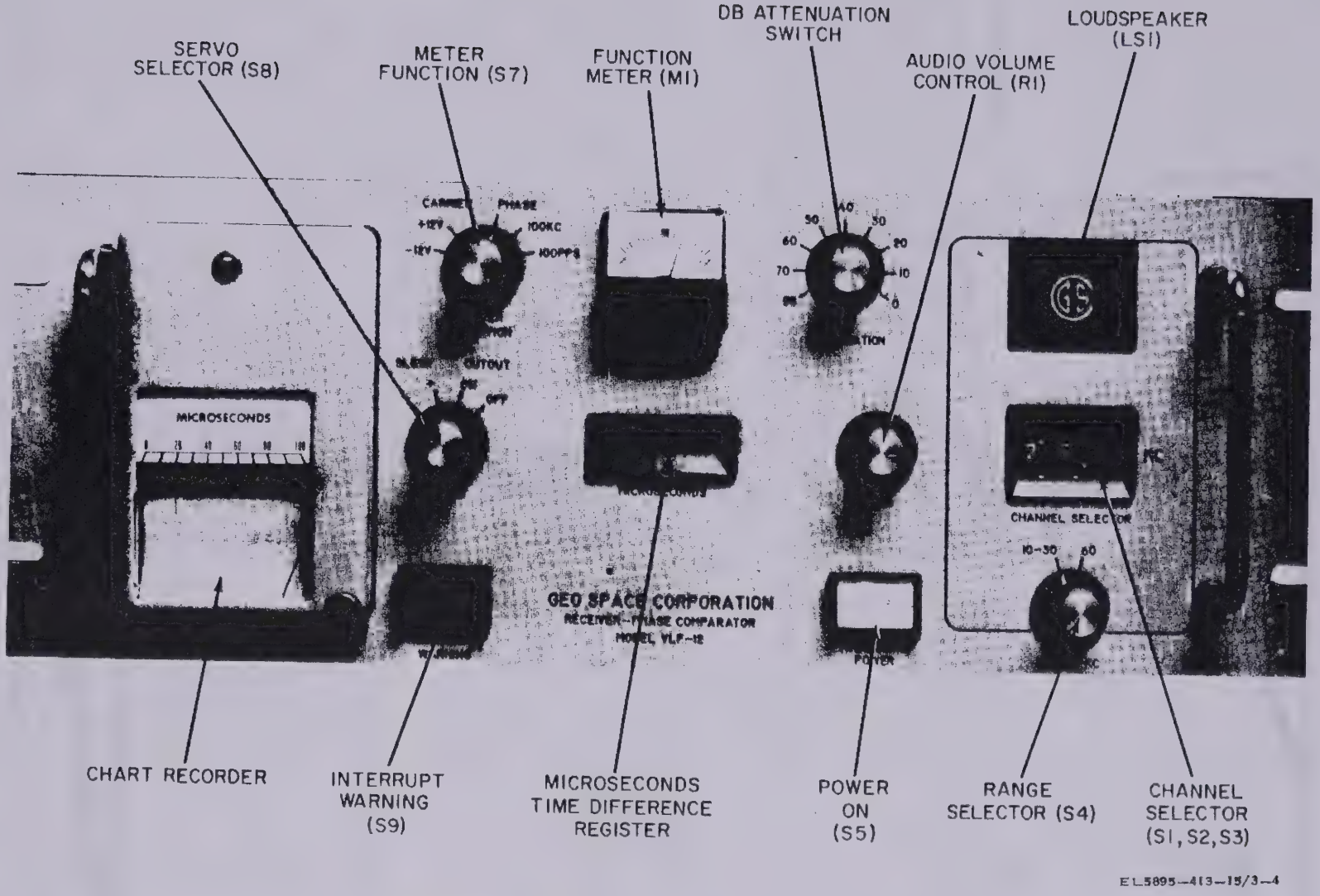



*Figure 2-2. VLF-12B receiver-phase comparator, front panel*

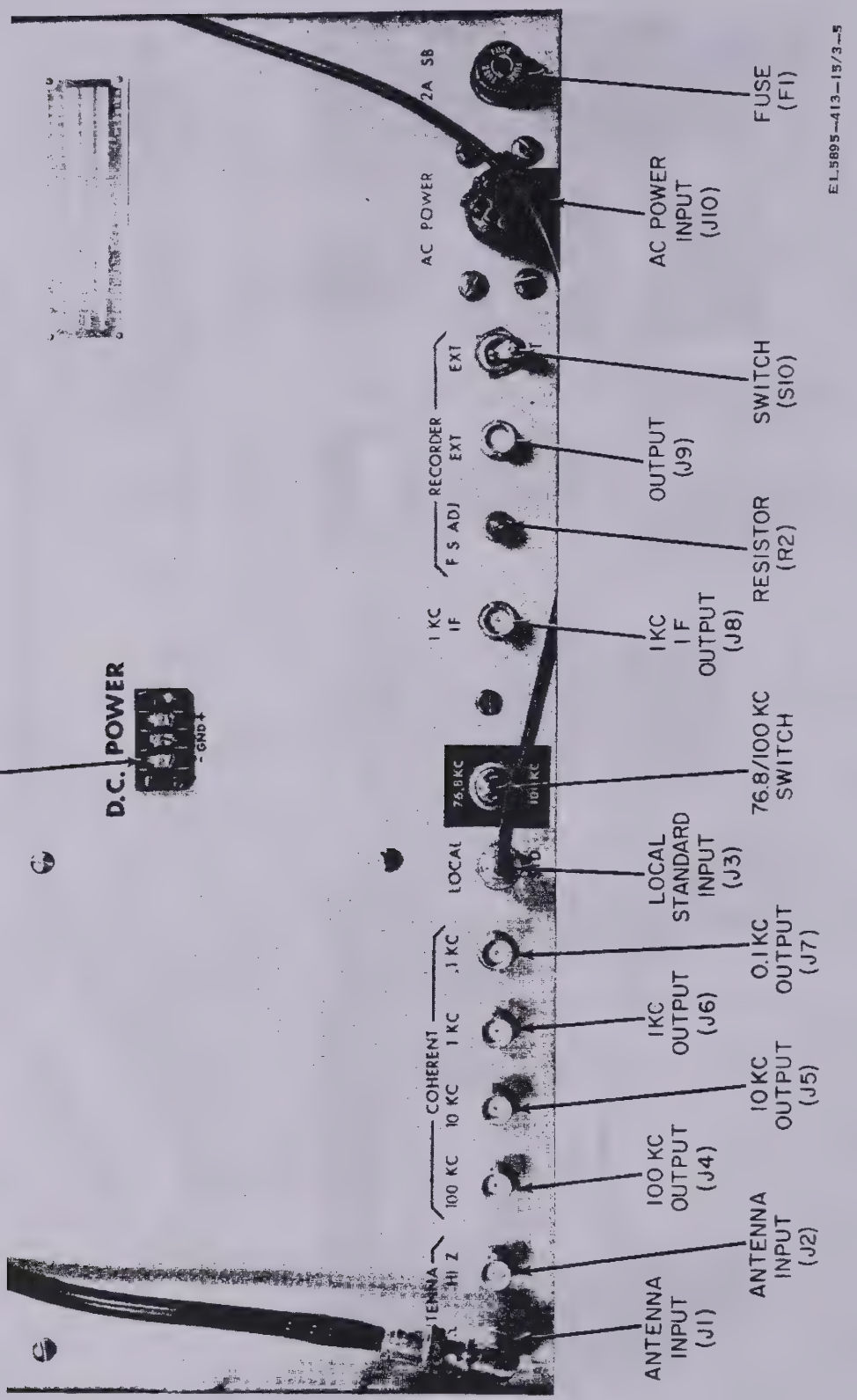



*Figure 2–3. VLF–12B receiver–phase comparator, rear panel*

# CHAPTER 3

# PRINCIPLES OF OPERATION

## Section I. GENERAL DESCRIPTION

### 3-1. Introduction

This chapter provides the principles of operation for the vlf-12B. The discussion progresses from a general block diagram level to a detailed description of the various circuits on a signal flow level. The block diagram discussion explains the general principles of operation, while the circuit description furnishes detailed functional theory of each element of the vlf-12B.

### 3-2. Functional Description

*a.* The underlying principle of the vlf-12B can best be understood by examination of the operation with input signals of 10, 20, and 30 kilocycles, respectively. Figure 3-1 is a simplified block diagram that demonstrates the phase-shift principle as it applies to each of the three frequencies wherein the vlf-12B is analogous to a single phase detector, operating at the selected incoming frequency. Since the servo system is a closed-loop device, it is difficult to consider under dynamic conditions. It is much easier to understand the operation if an input condition is stated and the proper response is assumed. Then after the servo is assumed to have come to rest, the resulting individual reactions through-out the system can be checked and if proved correct the entire response can be assumed to be correct.

(1) In case I, a 10-kc input signal with a convenient 10-microsecond step phase shift is assumed. After the servo system has achieved a null condition, the corrected 100-kc standard signal will have rotated a full 360° to compensate for the time shift of 10 microseconds. This will have occurred because when the vlf-12B is tuned to 10 kc, the corrected 100 kc is divided by 4.494 in the local oscillator synthesizer to provide the proper mixing frequency. As a result of this division process, the input to the 1st mixer is shifted in phase by 80.1°. Since both the incoming signal and the local oscillator have increased in phase, a resulting phase difference of 44.1° is realized at the first if. The mixing frequency required by the second mixer is 11.25 kc. This requires that the corrected 100 kc be divided by 8.889. This division ratio results in a positive phase shift of 40.5° at the oscillator input of the second mixer. Once again, since both phase relationships are increasing, a difference of 3.6° will result in the 1-kc IF signal. Since the corrected 100-kc standard has been divided by 100 to achieve the required 1-kc reference frequency for the phase detector, a 3.6° phase shift has resulted in this signal. Since both 1-kc inputs to the phase detector have shifted by 3.6°, a null condition has in fact been reached.

(2) In case II, when the vlf-12B is tuned to 20 kc, it can be seen that a 10-microsecond phase shift in the incoming signal will represent 72°. The servo system will move until a null has been reached, compensating for this time shift. This compensation is represented by 360° of the phase shifter. In this case the synthesizer will divide the corrected 100 kc by 3.101 with a resulting 116.1° phase shift in the local oscillator signal that produces a phase difference of 44.1° in the first if. Since the division factors of the second mixer injection signal and the phase detector reference signal remain the same, it can be seen that the resulting phase changes are 40.5° and 36°,

respectively. The output of the second mixer again has changed by 36°, and a null condition has been achieved by the servo system.

(3) In case III, a 30-kc signal is considered at the input of the vlf-12B and a 10-microsecond time shift is represented by 108° of the input signal. The synthesizer will divide the corrected 100 kc by 2.367 to produce a local oscillator phase shift of 1521°. The first mixer output will have a phase shift of 44.1° and logically, the remaining phase shifts are the same as in the previous two cases.

*b.* These three examples demonstrate that phase tracking has been achieved at all frequencies in the band of interest, and that the rotations at the phase shifter will represent the time error experienced in either the local standard or the incoming signal.

## 3–3. Simplified Block Diagram

*a. General.* The heavy black line in the simplified block diagram shown in figure 3–2 illustrates the main signal path through the actual vlf-12B. All major supporting functions are also represented. Although the block diagram shows a mechanical servo that utilizes a servo motor to provide the necessary phase shifting, the discussion that follows is applicable to vlf-12B's with either mechanical or electronic servo systems. The major functional sections are:

(1) Receiver section—consisting of the RF, 1st and 2nd mixer stages, IF amplifiers, audio amplifiers, and agc circuits.

(2) Comparator section—consisting of the servo phase detector, servo amplifier, servo cutout, servo motor phase shifter, and supporting logic circuits.

(3) Local oscillator synthesizer—consisting of the voltage-controlled oscillator (VCO), phase comparator, and the digital divider circuits and thumbwheel switches needed to synthesize the phase-locked local oscillator signal.

(4) Reference divider chain—a series of digital divider circuits that divide the corrected 100–kc signal from the phase shifter into internal reference signals and buffered outputs.

*b. Receiver Section.* For the discussion of the simplified block diagram (figure 3–2), it is assumed that a loop or whip antenna is connected to the 50-ohm input. The received signal is applied to an antenna matching transformer that couples the 50–ohm antenna to the 10-kilohm input circuit of a broadband RF amplifier. The transformer provides a voltage gain of $\sqrt{10{,}000/50} = 14.14$, or 23 db. From the rf amplifier, the signal is applied, depending upon selection, to either a 30-kc or 60-kc bandpass filter. At the 3-db points, the 30-kc filter has a bandpass of from 8 kc to 30 kc, as illustrated in figure 3–3, allowing coverage of the vlf frequencies in the 10-kc to 30-kc band. If the 60-kc bandpass filter is selected, a single channel at 60 kc is received. This filter has a bandpass of approximately 2 kc. From the filter, the signal is applied to an 80-db attenuator that is adjustable in 10-db increments by means of the front panel selector switch. The attenuated signal is then routed to a balanced mixer. The applied local oscillator frequency is always 12.25 kc (in 100-cps increments) above the incoming signal to provide a first intermediate frequency (IF) of 12.25 kc. The stages that follow are the 12.25-kc IF amplifiers and a crystal filter which has a center frequency of 12.25 kc and a pass band of ± 100 cps at the 3-db points. Response falls off rapidly to 80 db at 200 cps on either side of center. The if. amplifiers following the crystal filter are used to provide increased gain of the signal over a very narrow band. Following amplification at 12.25 kc, the signal is applied to the second mixer, where the 11.25-kc signal, obtained by multiplying a corrected 5 kc from the divider chain by 9 and dividing again by 4, provides a second intermediate frequency of 1 kc. From this point the 1-kc signal is further amplified and coupled to an output connector, to an audio amplifier, and to a 1-kc filter that restricts the bandpass to a nominal 50 cps.

*c. Comparator Section.* The output of the 1-kc filter is applied to the agc phase detector and to the servo phase detector. The agc signal from the phase detector controls the gain of the 12.25-kc if. amplifier and also operates the servo cutout that is used to automatically disconnect the servo system when the carrier level falls too low for reliable tracking. The servo phase detector compares the 1-kc carrier

# CHAPTER 3

# PRINCIPLES OF OPERATION

## Section I. GENERAL DESCRIPTION

### 3-1. Introduction

This chapter provides the principles of operation for the vlf-12B. The discussion progresses from a general block diagram level to a detailed description of the various circuits on a signal flow level. The block diagram discussion explains the general principles of operation, while the circuit description furnishes detailed functional theory of each element of the vlf-12B.

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*c. Comparator Section.* The output of the 1-kc filter is applied to the agc phase detector and to the servo phase detector. The agc signal from the phase detector controls the gain of the 12.25-kc if. amplifier and also operates the servo cutout that is used to automatically disconnect the servo system when the carrier level falls too low for reliable tracking. The servo phase detector compares the 1-kc carrier

signal with a corrected 1-kc signal obtained from the reference divider chain. Any phase shift error is detected and provides a signal to the servo amplifier, which operates a servo motor coupled to the phase shifter. The servo motor is also coupled, through a gear train, to a time difference register on the front panel that provides the readout (in microseconds) of the relative phase difference between the local frequency standard and the vlf carrier. The servo motor also drives a precision potentiometer that furnishes a phase error to the stylus of the chart recorder.

*d. Local Oscillator Synthesizer.* For a vlf transmission at 16.0 kc the required local oscillator frequency is 28.25 kc. In order to provide a frequency at multiples of 50 cps, instead of 100 cps, the voltage-controlled oscillator is operated at twice the local oscillator frequency, or 56.5 kc. When the digital thumbwheel switches are set at 16.0 kc, several functions are provided: first, a resistance network is selected which sets the VCO at approximately 56.5 kc; next, outputs from a digital divider are selected to obtain division of the 56.5-kc VCO frequency by a factor of 565 to achieve a synthesized 100-pps signal for use in the phase comparator. Here the synthesized 100-pps signal is phase-compared with a corrected 100-pps signal from the output divider chain. The + dc voltage at the output of the phase comparator is proportional to the phase difference and is used to phase-lock the VCO to 56.6 kc. Subsequently, the output of the VCO is applied to a flip-flop which divides the VCO by 2, providing a local oscillator frequency of 28.25 kc. Since the flip-flop is not directly in the phase-lock loop, an ambiguity of 180° can possibly exist, depending upon the initial state of the flip-flop. In order to eliminate the ambiguity, the flip-flop is reset to the proper state by a pulse obtained from a phase gate that compares the corrected 50 pps from the divider chain, the synthesized 100 pps from the synthesizer, and the output of the flip-flop.

*e. Output Divider Chain.* The divider chain consists of three divide-by-10 cards which provide 10 kc, 1 kc, and 0.1 kc phase-corrected to the vlf carrier through buffered outputs. In addition, these circuits provide 50 kc, 5 kc, 1 kc, and 100 pps for use by the receiver section.

## Section II. DETAILED BLOCK DESCRIPTION

### 3-4. General

Detailed block diagrams pertaining to the following discussions are shown in figure 3-4. Individual blocks are identified with the module card reference designators. Although these sections were discussed in general terms in paragraph 3-3, a more detailed description of the complicated or unusual elements of the vlf-12B is provided in the following paragraphs.

### 3-5. Local Oscillator Synthesizer

The voltage-controlled oscillator (VCO) is set at twice the desired local oscillator frequency and is controlled by two separate phase detectors, a "fast-loop" and a "slow-loop" phase detector. A thumbwheel switch and a resistance network in series with the fast loop set the coarse range for the VCO. The fast-loop phase detector, with its low gain, has a large "capture range" and initially acts to bring the VCO on frequency. Since the fast-loop detector has low gain, there is a tendency for the VCO to "hunt" and produce jitter; however, the slow-loop phase detector, with its high gain and long time constant, keeps the VCO on frequency without jitter.

*a.* The reference inputs to both phase detectors are corrected 100-pps signals from the divider chain. Both have a 50% duty cycle, but the fast-loop reference signal is advanced one millisecond with respect to the slow-loop reference signal. These reference signals are compared in the separate phase detectors with the 100 pps from the synthesizer, and the resultant error signal is applied to the VCO. The 50% duty cycle, 100-kc reference signals for this purpose are obtained by applying a 100-pps signal with a 40% duty cycle from module A23 (MOD-10 divider) to both synthesizer phase detector OR gates A13. (Refer to figure 3-5 for the detector waveforms.) The decimal "3" output of A23 is applied to

the second input of the OR gate in the fast-loop phase detector, while the decimal "8" output of A23 is applied to the second input of the OR gate in the slow-loop phase detector. The output of each OR gate is thus a 100-pps reference signal with a 50% duty cycle but with the fast-loop reference advanced one millisecond from the slow-loop reference.

*b.* In the fast-loop detector, the reference signal from the OR gate is applied to a ramp generator that produces an integrated wave (F, figure 3-5). The synthesized 100 pps is applied to a 500-microsecond one-shot multivibrator, A13, that is used at the ramp generator to stop the ramp while it is being sampled. The 500-microsecond pulse is also routed to a sample-and-hold gate and phase detector, A13, where it is compared with the buffered level from the ramp generator. The error output of the phase detector is integrated and applied through a high-impedance, unity-gain amplifier, then through the resistance network connected with the thumbwheel switches to VCO A6. The high-impedance, unity-gain amplifiers following the ramp generator and integrator of the phase detector are used to prevent loading of these two stages.

*c.* In the slowloop phase detector, the square-wave reference from the OR gate is applied through an inverter and complementary emitter follower to phase detector A12, where it is compared with 100 pps from the synthesizer. Any error voltage from the phase detector is integrated with a time constant that is much greater than the time constant of the corresponding integrator in the fast-loop phase detector. The integrated signal is then applied to VCO A6.

*d.* The synthesized 100 pps is obtained by applying the output of the VCO that is operated at twice the desired local oscillator frequency to phase splitter A6, which provides two outputs that are phased 180° apart. The 0° output is connected to a series of digital dividers (A7 through A10), and the 180° output is applied to the fixed and variable gates. The first two dividers (A7, A8) are MOD-10 modules with decimal outputs, while the third (A9) is a MOD-3 module. The hundreds decimal conversion gates for the MOD-3 module are located on module A10. Module A7 provides units division, while A8 and A9 provide tens division and nundreds division, respectively.

*e.* The following example illustrates the basic operation of the synthesizer. To receive a vlf signal at 24.0 kc, the required local oscillator (L.O.) frequency is RF + IF = L.O., or 24 kc + 12.25 kc = 36.35 kc. The VCO, operating at twice the L.O., generates 72.5 kc. This can be considered to be (2 RF + 2 IF.), which in this case would be 2 x 24 kc + 2 x 12.25 kc, or 72.5 kc. In order to produce 100 pps, the VCO divisor would have to be:

$$\frac{2RF}{100} + \frac{2IF}{100}, \text{ or } 2(240) + 245 = 725$$

The 245 portion of the divisor is a constant for all channels and is recognized in a fixed 245 AND gate, while the variable portion is recognized in a variable count gate. The fixed gate receives its input from the outputs of the dividers (200 count from A9 and A10, 40 count from A8, and 5 count from A7). An inhibit pulse is also connected to the fixed gate from the inhibit flip-flop located on module A9. The inhibit pulse stops the fixed gate at the end of the 245 count and opens the variable gate. The variable gate receives a count from the proper divider outputs through selected thumbwheel switch positions. It must recognize the 240 count twice since the output of the gate is divided by two. At the end of the second 240 count, when the variable gate is inhibited by inhibit flip-flop A9, the fixed 245 gate is opened.

*f.* For the gates to recognize the proper count, a VCO signal from the 180° output of the phase splitter is applied to the input of both the fixed and variable gates. This signal supplies the set and reset pulses to the inhibit flip-flop at the end of the proper count. The reset pulse, at the end of the 245 count, is gated to complementary emitter follower A10 and to inhibit flip-flop A9, while the set pulse, at the end of two 240 counts, is gated to a divide-by-two flip-flop that actuates the inhibit flip-flop. The outputs of the fixed and variable gates are also connected to an OR gate that actuates a chain consisting of a nominal

2-microsecond one-shot, a reset driver, and reset gates. The reset gates set the dividers to ZERO at the end of the fixed 245 count and again at the end of the proper variable gate count, in this case after two 240 counts. Thus, the synthesized 100 pps is obtained from the output of the complementary emitter follower, which follows the fixed count gate in module A10, for use in the fast and slow-loop phase detectors and in the ambiguity elimination gate as previously explained.

### 3–6. Second Mixer

*a.* A corrected 5-kc signal is obtained from the divider chain. This is applied to an X9 multiplier, which brings the frequency to 45 kc. This 45-kc signal is applied through a buffer and through two successive divide-by-two flip-flop stages which divide the 45 kc to 11.25 kc. The 11.25-kc signal is mixed to obtain the 1-kc second IF signal.

*b.* The output from the second mixer is applied to two circuits. The first circuit is a 1-kc if. amplifier that produces an output audio signal and a 1-kc monitor output for time markers ("ticks"). The second circuit is another 1-kc if. amplifier with a nominal 50-cps bandwidth. The output of this amplifier is applied to a symmetrical clipper stage that preserves signal symmetry and clips any noise present at that point. The output of the clipper is then coupled through a second 1-kc if. amplifier and a complementary emitter-follower stage to the servo and agc phase detectors located within the servo system.

### 3–7. Mechanical Servo System

*a.* A detail block diagram of the single-speed mechanical servo system is shown in figure 3–6. Since synchronous phase detection is employed by the vlf-12B, the following discussion can be better understood by reference to figure 3–7.

*b.* From the reference divider chain, synchronous 1-kc signal pulses, which are separated by 90° in phase, are compared with the 1-kc if. signal at the servo and agc phase detectors. Figure 3–7 illustrates the relative positions of the two sampling pulses and the 1-kc IF signals. Examination of the waveforms shows that retarding the servo sample pulse produces a positive voltage, while advancing the phase sample pulse produces a negative voltage. This plus or minus voltage is integrated to produce a dc level that is proportional to the phase error. The dc signal is chopped at approximately 1 kc and coupled to an emitter follower that is used to prevent loading of the integrator. Chopping provides a signal that can be ac-coupled to the servo amplifiers, thereby helping to maintain stability in the servo amplifiers. The signal is then connected through emitter followers to a synchronous demodulator circuit that restores the signal to its original plus or minus dc level. The complementary-type demodulator is driven by complementary 1-kc pulses from the same astable circuit that drives the chopper. The dc error signal from the demodulator is then applied through the contacts of a servo cutout relay and used to drive the servo motor. The servo cutout is normally closed, but opens to disconnect the servo motor whenever the carrier level is too low for reliable tracking. A selector switch on the front panel provides a means of manually slewing the servo motor to bypass the servo cutout. The servo cutout relay is operated by the agc voltage from the agc amplifier circuit. An additional set of contacts on the servo cutout relay operates an INTERRUPT WARNING indicator to indicate loss of the carrier and that the servo is disconnected.

*c.* The servo motor is mechanically coupled to a gear box that utilizes a X10 gear ratio to drive a digital time difference register, a divide-by-10 gear ratio to drive a precision recorder potentiometer, and a 1:1 ratio to drive a 100-kc phase shifter. At the 100-kc phase shifter, a signal from the local standard input is shifted in phase to be coherent with the vlf carrier. The standard frequency input from the local reference is usually 100 kc, but an optional 1-mc provision is available. From the input connector, the standard input is clipped and coupled through a series of amplifier filters and a phase splitter to the phase shifter circuit. Clipping limits the input to the amplifiers to prevent overdriving and also provides a square wave for operation of the 1-mc to 100-kc MOD–10 option, when utilized. The

coherent 100-kc signal is amplified and squared through a Schmitt trigger circuit and used to drive the divider chain.

*d.* The agc detector is gated with a 1-kc pulse signal that is in quadrature (90°) to the signal used in the servo phase detector. The quadrature signal is obtained by applying three 1-kc signals from the MOD-10 to an OR gate. The output of the OR gate is a 1-kc pulse, 90° in phase relative to the servo signal. As shown in figure 3-7, when the servo reaches a null, the agc reaches a maximum. Since the agc detector provides an output in all four quadrants, the servo cutout relay is activated regardless of the position of the phase shifter when the receiver is energized or switches to a new frequency. This actior prevents the servo cutout relay from being de-energized, thus preventing the phase shifter from acquiring track when the servo phase detector is at 90°. The quadrature detection is accomplished by applying the output of an emitter follower (A18) to a detector and filter and on the one input of an OR gate (A15), providing agc at 90° and 270°. The agc at 0° is obtained directly from the agc circuit and applied to the OR gate, while agc at 180° is obtained by inverting the agc output and applying it to the OR gate. Thus, agc is obtained in all four quadrants.

## Section III. INDIVIDUAL CIRCUIT ANALYSIS

### 3-8. Basic Signal Circuits

*a. General.* A discussion of the individual circuit modules used on the standard vlf-12B is explained in this section. Some of the circuits are located on the printed circuit cards, some on the vlf-12B chassis. It is necessary to refer to figure 3-8, the vlf-12B schematic diagram, for circuits located on the chassis and to figure 3-9, a top view of the vlf-12B, for the locations of all circuit modules and assemblies.

*b. RF Amplifier and First Mixer (A1).* Figure 3-10 shows the schematic diagram for the rf amplifier and first mixer (A1).

(1) The 60-kc filter consists of transistor Q9, resistors R22 and R23, capacitors C19, C20, and C21, inductor L8, and relay K1. The output of rf amplifier Q2 is connected from the collector through capacitor C4 and the input filter to the attenuator. This attenuator provides 80 db of attenuation in 10-db steps and is controlled by a selector switch on the front panel.

(2) A long-wire antenna would connect to the HI Z input representing 10 kilohms at pin 30, and a loop or whip antenna would connect to the 50-ohm input at pins 26 and 28. Transformer T1 provides an impedance match of 50 ohms to 10 kilohms with a corresponding gain of 23 db to the input signal. Transistor Q2 and associated circuitry form a broadband untuned rf amplifier. Decoupling of power supply voltages is accomplished by L1, L2, C3, and C5. Bias for Q2 is obtained through resistors R4 and R5 and bypassed by C2. Negative feedback is provided by resistor R7, which limits the gain of the stage to slightly over unity. The output of the rf amplifier is connected through C4 to an 8 to 30-kc bandpass filter, FL2, or to the 60-kc bandpass filter with a nominal 2-kc bandwidth. Transistor Q3 and its associated components drive the 600-ohm input impedance of transformer T2 with approximately unity gain. Power supply decoupling for this stage is accomplished by L3 and C6. Similar decoupling is utilized throughout the receiver circuits.

(3) Transistors Q4 and Q7 make up a complementary balanced mixer circuit. This circuit is designed for signals as large as 1 volt rms, and its dynamic range is greater than 90 db. Complementary balanced input is provided by transformer T2, while the local oscillator input is fed to the bases of the transistor through C11 and an appropriate resistor network comprising R11 through R13 and R15. Capacitors C9 and C10, inductor L5, and resistor R16 make up a series resonant trap, tuned to 12.25 kc and used to prevent harmonics of the local oscillator, near the first if. frequency, from appearing at the input to the mixer. The output of the mixer is tuned by C13, C14, and L6 to the difference frequency

of the input and local oscillator frequencies, producing the required 12.25-kc first if. The first if. at 12.25 kc is amplified by Q8 and coupled to a 12.5-kc crystal filter, FL1, providing a bandpass at the 3-db points of 200 cps. The bandpass characteristics of the crystal filter, FL1, are shown in figure 3–11.

*c. IF and AGC Amplifier Module (A2).* The schematic diagram for the IF and agc amplifier module (A2) is figure 3–12. The output of the 12.25-kc crystal filter is coupled through C1 (pin 7) to the base of Q1, the first IF amplifier stage. The emitter of Q1 is connected through R3 to Q8, which controls the gain of the first IF amplifier by acting as a variable impedance in the emitter circuit thus providing a varying negative feedback. Transistor Q8 normally is saturated and represents a low impedance to the emitter of Q1, thus allowing maximum gain of that stage. The agc voltage from the quadrature detector is amplified by Q5 and used to control the servo cutout circuit in the servo system. The output of Q5 is also integrated by C13 and R20, then further amplified by the Darlington circuit consisting of Q6 and Q7. The dc current from this amplifier is used to control agc transistor Q8. An increase in agc current reduces the collector current of Q8, which increases the effective impedance in the emitter circuit of Q1 and reduces the gain of that stage. The agc circuit provides a dynamic range in excess of 40 db, thus resulting in large signal-handling capacity at the input to the first IF amplifier. Transistors Q2 and Q4 are emitter followers that prevent loading of the tuned circuits of first IF amplifier Q1 and second IF amplifier Q3. The output of emitter follower Q4 is connected through pin 18 to the normal mode second mixer.

*d. Second Mixer Assembly (A4).* The schematic diagram of the second mixer is shown in figure 3–13. The IF input of 1.25 kc at pin 2(B) is coupled through C7 to the base of Q4, an emitter follower. The output of Q4 is used as one input to Q6, a bi-directional mixer stage. The second input to Q6 is obtained from amplifier Q5, which receives an input of 11.5 kc through C8 from pin 4(D). The 11.25-kc signal is obtained by multiplying a 5-kc signal from the chain divider by four, then dividing by nine. The 5-kc input at pin 30(j) is coupled through C1 to the base of Q1, an emitter follower. The resonant tank circuit of L1 and C3, between A1 and emitter-follower Q2, is tuned by the manufacturer to 45 kc. Resistors R6 and R5 provide bias for Q2, whose output is then coupled to Q3. Transistor Q3 is a saturated amplifier with its collector clamped to +6 volts by diode CR1. The output of Q3 is coupled through pin 22(Z) to two flip-flop circuits on module A5.

*e. Three Flip-Flops and Gates Module (A5).* Figure 3–14 is a schematic of the three flip-flops and gates module, A5. The first two bistable circuits are used to divide the 45-kc signal from the normal mode second mixer down to 11.25 kc, while the third bistable circuit is used to divide the corrected 100-pps signal from the divider chain down to 50 pps. The 50 pps provides the gating signal for the ambiguity gate circuit comprised of Q7 and Q8. This circuit acts as a three-input AND gate with the inputs present at pins 31(K), 29(H), and 26(D). The input at 31(K )is a 100-pps signal from the synthesizer, while the input at 29(H) is the corrected 50-pps signal from the third flip-flop on the same card. The third input at pin 26(D) is obtained from the collector output of the divide-by-two flip-flop that is used to divide the VCO output down to the proper local oscillator frequency. Since the flip-flop used to divide the VCO frequency can be in either one of two possible states, an ambiguity can exist. If the bistable circuit is in the proper state when first energized or when switched to another frequency, the input at pin 26(D) inhibits the gate, and no output reset pulse is produced to reset the flip-flop. If the bistable circuit is in the opposite state, is ouput enables the gate, and a reset pulse from the collector of Q8 is coupled through C7 and CR16 back to the bistable circuit, resetting it to the proper state.

*f. Local Oscillator and VCO Module (A6).* A schematic diagram of the local oscillator and voltage-controlled oscillator (VCO) is shown in figure 3–15.

(1) The VCO is a modified, free-running (astable) multivibrator. Transistors Q4 and Q5 with their associated components comprise the basic astable circuit. The frequency

of the circuit is controlled by C11, C12, Q6, Q7, and the resistance network of R16 through R21. Diodes CR10 and CR11 are used as an OR gate to prevent the astable circuit from not starting if Q4 and Q5 were to conduct the same amount simultaneously. If this condition should occur, a negative voltage is coupled through voltage divider R22 and R24 to the base of Q8, causing it to conduct heavily, which sufficiently unbalances the astable multivibrator to make it start.

(2) When the thumbwheel switches are set to a selected channel, the coarse frequency of the astable multivibrator is set by the resistance network connected to the thumbwheel switches through pins 4(D) and 2(B). Transistors Q6 and Q7 act as variable impedances that change the frequency of the astable multivibrator and phase-lock to the VCO to the exact frequency. The impedance of Q6 and Q7 varies as a function of the conduction through them; that is, at saturation their impedance is a minimum, but the impedance increases as the current is decreased. The conduction of these two transistors is precisely controlled by the control voltage from the fast-loop phase detector in their emitter circuits and by the control voltage from the slow-loop phase detector in their base circuits. The slow-loop control voltage at pin 30(j) is connected through R12 to their bases, while the fast-loop control voltage at pin 5(E) is connected through resistance network R16–R21 to their emitters. The output of the VCO is obtained from the collector of Q4 and applied to bistable circuit Q2 and Q3, which divides the VCO frequency by two to produce the required local oscillator frequency. This bistable circuit can produce an ambiguity, depending upon the state that occurs when the flip-flop is first energized.

(3) When the flip-flop is in the proper state, Q3 is conducting at saturation and the collector of Q3 is approximately at ground potential. This low voltage is coupled through pin 13(P) to the ambiguity gate in module A5, inhibiting it. If the Q3 collector is at a high potential, the gate is enabled and couples a reset pulse through pin 11(M) to the base of Q3, thus resetting it to the proper state. The local oscillator output from Q2 is coupled through C1 and R3 to buffer amplifier Q1. The output of Q1 is then connected through pin 3(C) to the mixer in module A1.

(4) The output from the collector of Q5 is coupled to phase splitter Q9, which produces VCO outputs with 180° phase relationships. The 0° output at pin 28(F) is connected to the MOD–10 synthesizer divider, where it is divided down to 100 pulses per second. The 180° output at pin 29(H) is applied to the inputs of both the fixed and variable count gates to act as a recognition pulse for the proper count from the synthesizer.

*g. MOD–10 Counter Circuits (A7, A8, A21, A22, and A23).* Modules A7, A8, and A21 through A23 are standard MOD–10 counter circuits. Figure 3–16 is a schematic of a typical MOD–10 counter circuit, and the following description is for a typical MOD–10 counter with decade outputs.

(1) The counter is basically composed of four flip-flops, utilizing the necessary feedback to produce a natural divide-by-10 counter. The card has both the true and false outputs of each flip-flop brought out to the connector. A diode matrix, required to provide a decimal output, is also included on the card, and each decimal output is tied to an individual pin on the connector. It is important to note that the diode matrix is complete with the exception of the pull-up resistors necessary to obtain the basic AND function. This means that an external pull-up resistor is required to obtain any one of the decimal outputs.

(2) Since the basic flip-flop can take a random stable state, assume that transistor Q1 is conducting and Q2 is off. Since Q1 is in the saturated condition, its collector is at approximately +0.15 volt, while the collector of Q2 is clamped approximately +6 volts due to the conduction of CR3. This +6 volts causes the base of Q1 to be biased in the forward direction through cross-coupling resistor R3. The base of Q2 is back-biased by the –12 volts supplied through R2. The back-bias network provides basic immunity to high temperature. When a pulse arrives at the input of the MOD–10 counter (pin A), it is steered to either Q1 or Q2 depending on the voltage

level at the junction of R5, CR1, and C1, and the junction of R6, CR2, and C2. In the case just described, Q1 is conducting; therefore, its collector is at approximately 0 volts. This supplies approximately 0 volts bias at the junction of R5, CR1, and C1. The volts bias allows the incoming negative pulse to conduct through CR1 and drive Q1 to the off condition. Conversely, Q2 originally was nonconducting; therefore, its collector was at +6 volts, which biased the junction of R6, CR2, and C2 to a positive voltage. The positive voltage is a back bias for CR2; thus, the negative pulse is not conducted to Q2. After the condition of the flip-flop is reversed by the previous incoming negative transition, the bias conditions at the two junction points are also reversed. The next negative pulse is steered to the opposite base. In this manner, the first flip-flop of the MOD-10 counter divides the incoming pulse stream by two. The output of the first flip-flop is tied to the toggle input of the second flip-flop through the gate circuit consisting of CR20, CR21, and R34.

(3) Assuming that the MOD-10 counter starts in the reset condition (that is, Q2, Q4, Q6, and Q8 conducting), the gate made up of CR20 and CR21 is enabled, and the gate made up of CR18 and CR19 is disabled. This can be shown by examining the enabling signal supplied through CR19 and CR21, which is generated by the positive voltage level supplied by Q7. Since Q7 is nonconducting, this level is at +6 volts, supplying a positive bias through CR19 and R35 to diode CR17. This positive voltage is used to back-bias CR17, keeping the negative transitions from passing through C9 to the last flip-flop. The positive voltage resulting from Q7 is also applied to CR21, keeping the AND gate comprised of CR20 and CR21 continually enabled so that the negative transitions from the first flip-flop are continously applied to the toggle input of the second flip-flop. This condition is maintained until the circuit reaches a count of nine, which is represented by a conducting condition of Q1, Q4, Q6, and Q7 and a nonconducting condition of Q2, Q3, Q5, and Q8. The fact that Q1 and Q7 are now conducting results in the application of a zero level voltage to the junction of CR18 and CR19, enabling the next negative transition to be passed through CR17 to reset the fourth flip-flop to a ZERO condition. The zero level voltage applied to CR21 disables the AND gate made up of CR20 and CR21 and inhibits the next negative transition from being carried to the second flip-flop. In this manner, all four flip-flops are placed in the ZERO condition, thus providing a natural reset to decimal zero on the tenth pulse. Examining each of the diode gates shows that the binary conditions are satisfied in each gate to provide a decimal count from 1 through 10. As previously mentioned, it is necessary that a pull-up resistor be added external to the card to make the AND gates operate in the proper manner.

*h. Four Flip-Flops Module (A9).* Figure 3-17 is a schematic diagram of the four flip-flops module, which is designed to supply the maximum number of flip-flops per card with the minimum number of gates necessary to accomplish normal binary operation. Four circuits are available on the card, each having a single complete pulse gate on each side of the flip-flop.

(1) The first two flip-flops (Q1-Q4) are connected to gates on module A10 to make up a MOD-3 module with decimal outputs that provide the hundreds count for the synthesizer. The third flip-flop (Q5-Q6) is the inhibit circuit for the fixed and variable count gates. The flip-flop consisting of Q7 and Q8 is used to divide the variable count gate output by two, and its output is used to reset the inhibit flip-flop. A flip-flop circuit is a bistable multivibrator; that is, it can be stable in either of two states. In each state one transistor is on while the other is off. With an input trigger pulse on one side, the circuit is switched into one of the stable states; with an input pulse on the opposite side, the circuit is switched into the other stable state. Each time switching occurs, an output level change is provided.

(2) To examine the circuit operation, assume that Q1 is saturated and Q2 is cut off. Since Q1 is saturated, its collector is at ap-

proximately +0.15 volt. The collector of Q2 is clamped at approximately +6 volts due to the conduction of CR5. The base of Q1 is biased in the forward direction by coupling resistor R5. The base of Q2 is back-biased by the -12 volt supply through R4. This back-bias provides the circuit with stability at high temperatures. When an input pulse is applied to pin D, it is differentiated by C1 and R1. Diode CR1 allows only the negative portion to be applied to the base of Q1. The negative pulse overcomes the forward bias, increasing as the collector current decreases. The increasing collector voltage is coupled through R6 to the base of Q2, causing it to conduct and thereby decreasing its collector voltage. During the rapid transition period when both transistors are conducting, the conduction of one transistor is decreasing while the other is increasing. The changing collector voltage of each transistor is applied back to the base of the other transistor. The regenerative feedback process continues until Q1 is cut off and Q2 is saturated. The positive collector swing of Q1 is clamped at approximately +6 volts by CR6. The circuit remains in this state until a negative pulse arrives at the base of Q2, causing it to revert to its original state.

(3) The output, taken from either collector, is a unit step voltage for each pulse at the input. A binary divider can be obtained by connecting pin B to the collector of Q1 and pin E to the collector of Q2, then tying pins C and D together as the triggering input.

*i. One-Shot and Reset (A10).* The schematic for this module is shown in figure 3-18. The circuits provided include a five-input variable count AND gate, a five-input fixed count AND gate, two-input OR gates, a nominal 2-microsecond one-shot, a reset driver, ten output reset gates, and a complementary emitter follower.

(1) The five-input variable count AND gate consists of diodes CR12 through CR16 and pull-up resistor R18. The five-input fixed count AND gate is made up of diodes CR17 through CR21 and pull-up resistor R21. Resistors, R16, R17, R19, R20, and R23 serve as pull-up resistors for five fixed decade output gates located in the units and tens synthesizer divider modules.

(2) The set inhibit pulses and the count recognition pulse inputs for the fixed count gate are connected to pin 6(F). The reset inhibit pulse and the count recognition pulse inputs are connected to pin 7(H). The variable count gate inputs at 9(K), 10(L), and 11(M) from the synthesizer dividers are selected through the thumbwheel switches, while the fixed count gate inputs at 4(D), 5(E), and 22(Z) are obtained directly from the synthesizer dividers. A fixed count of 245 is obtained by gating a 200-count signal from the hundreds divisor (MOD-3) through pin 22(Z) to diode CR21; the 40-count signal from the tens divisor (MOD-10) through pin 5(E) to diode CR18; and a 5-count signal from the units divisor (MOD-10) through pin 4(D) to diode CR17. The output of the fixed count gate is coupled through differentiator C2 and R6 to diode CR2, the input of the count set OR gate, and to the bases of complementary emitter-follower transistors Q4 and Q5. The other input of the count reset OR gate is applied from the output of the variable count gate through differentiator C1 and R1 to diode CR1. Whenever the OR gate receives a pulse from either the fixed or variable count gate, indicating the completion of the proper count for the gate, it triggers the 2-microsecond one-shot (Q1 and Q2) that activates reset driver Q3 for the purpose of resetting all three dividers to zero.

(3) The output pulse width of the conventional one-shot multivibrator is controlled by C3 and R4. Diodes CR3 and CR4 clamp the collectors of Q1 and Q2 to +6 volts. Resistors R7 and R11 provide reverse biasing from -12 volts. The output from the collector of Q1 is coupled to the reset driver, Q3.

(4) The reset driver is a saturating transistor switching circuit with the collector clamp to +6 volts through CR5. It inverts the one-shot pulse and supplies the drive current for the 10 reset diodes, CR22 through CR31.

(5) The output of the complementary emitter follower (Q4 and Q5) is a synthesized 100 pps derived from the VCO through the synthesizer. It is used as a reference signal

for the synthesizer phased detectors and for the ambiguity gate.

(6) Diodes CR6 through CR11 and pull-up resistors R14 and R15 make up the decimal conversion gates for hundreds division (MOD-3).

*j. Slow- and Fast-Loop Synthesizer Phase Detectors (A12 and A13).* The schematic drawing for the slow-loop phase detector is shown in figure 3-19.

(1) The synthesized 100-pps reference signal is coupled to the bases of Q4 and Q5 through pin 12(N), C3, and R14. The two corrected 100-pps reference signals from the divider chain are coupled to the emitter of Q4 and the collector of Q5 after having been combined in the loop OR gate (CR1 and CR2), the inverter (Q1), and the complementary emitter follower (Q2 and Q3). The error signal output from the collector of Q4 and the emitter of Q5 is integrated by R16 and C4, a long time constant, and is coupled to the VCO through the unity gain amplifier (Q6 and Q7).

(2) The dc error signal at the base of Q6 is a function of the phase difference between the input signals. It is transferred without attenuation through Q6 and CR5 to the collector of Q7. Zener diode CR6, with a nominal 5.1-volt breakdown level, helps to establish a quiescent level of approximately -5 volts for the error signal that is routed through the voltage divider consisting of resistors R19 and R20, and potentiometer R22 from the -12 volt source. Potentiometer R22 is used to compensate for any tolerance variations of components. The error signal that emerges at pin 30(J) for application to the VCO (A6) is a dc level varying above and below the -5 volt quiescent level.

(3) A schematic drawing for the fast-loop phase detector is shown in figure 3-20. The phase detector circuit (Q12 and Q13) is similar to the slow-loop detector. The synthesized 100-pps reference signal triggers a nominal 500-microsecond one-shot multivibrator (Q1 and Q2) that provides the pulse width required by the hold gate. The one-shot output is coupled to an emitter follower (Q3). The buffered output appears at the sample and hold gate (Q11), with Q11 acting as a constant-current source. The signal is applied to the bases of phase detector transistors Q12 and Q13. Concurrently, the corrected 100-pps reference signals with the 10% and the 40% duty cycles are OR-gated through CR2, CR3, and R13 to obtain the required 50% duty cycle signal, which is inverted by Q4 and is coupled to Q5 and Q6. The ramp generator is composed of transistor Q5 and Q6 and an integrating capacitor, C3.

(4) At approximately 1 millisecond after C3 begins to charge, the ramp is stopped for 500 microseconds by means of the buffered pulse from the one-shot multivibrator applied to the base of Q5. The charging of C3 continues after the 500-microsecond interval has elapsed. The resulting ramped wave, now containing a 500-microsecond plateau that coincides in time with the output of the one-shot, is applied through a high input impedance unity gain amplifier consisting of Q7 through Q10 and associated components to the phase detector. It is compared with the 500-microsecond pulse derived from the synthesized 100-pps, and the resulting error signal is related to the ramp signal amplitude at the time of the plateau, which in turn is a function of the phase shift between the input signals. Integration of the error signal is accomplished by the network consisting of C4 (4.7 $\mu$f), R35 (10 megohms), and R36. The integrated error is applied to a unity gain amplifier (Q14 and Q15) and a subsequent emitter follower to obtain isolation from the integrator and the requisite power amplification.

*k. Servo and AGC Phase Detector (A15).* The schematic drawing for the phase detector is shown in figure 3-21. The module contains a complementary servo phase detector (Q1 and Q2), a bidirectional agc phase detector (Q7), an agc input reference OR gate and amplifier (CR1, CR2, CR3, and Q6), complementary servo reference input amplifiers (Q3 and Q4), a unity gain inverter (Q8), a detector and filter (Q5), and an agc quadrature output OR gate (CR4, CR5, CR6).

(1) The purpose of the servo phase detector is to develop an error signal that is a

function of the phase displacement between the corrected 1-kc reference derived from the local frequency standard and the 1-kc second intermediate frequency signal from the receiver section.

(2) Complementary-corrected 1-kc reference signals are applied through saturating inverter amplifiers Q3 and Q4 to the bases of phase detector transistors Q1 and Q2. The negative reference is applied to Q1, the positive reference is applied to Q2, and the constant-amplitude 1-kc second IF signal is directly coupled to the collectors of Q1 and Q2. The resulting dc error signal is obtained at the emitters of Q1 and Q2, and is coupled through R2 to an external integrating capacitor, C5. The divider network consisting of R10, R11 (a potentiometer), and R12 is used to establish a dc reference level for a balanced error output.

(3) Since a relatively constant second IF amplitude is needed for accurate phase tracking, the gain of the receiver must be accurately adjusted for signal strength variations within a 40-db range. Therefore, the purpose of the agc phase detector is to develop an automatic gain control signal that is derived only from variations in vlf carrier signal strength. To accomplish the objective of sensing carrier strength, but rejecting the potential effects of noncoherent atmospheric noise, involves application of a technique for coherent signal detection capable of producing an agc signal under all phase tracking conditions.

(4) Figure 3-6 illustrates the quadrature detection scheme used to generate the combined agc signal. In particular, it shows that the 90° and 270° quadrants of detection are obtained from the servo phase detector and are combined in an OR gate with signals from the agc detector corresponding to the 0° and 180° quadrants. Under normal phase tracking conditions, i.e., when the servo phase detector is at null, agc detector Q7 will develop a signal which is the product of the 1-kc IF input applied to the collector and a corrected 1-kc reference signal (derived from selected outputs of MOD-10 divider A22) that is displaced 90° from the servo phase detector reference. The output of Q7 is integrated by the network consisting of R24 and C8, and is applied to OR gate input diode CR5 and through CR7 to the input of unity gain inverter Q8. The output of the inverter is applied to OR gate input diode CR6, and its phase is 180° with respect to the signal at diode CR5.

(5) The servo phase detector-integrator-amplifier-detector/filter chain is connected to OR gate input diode CR6, but since the servo phase detector is at null, no signal is provided. Thus, during normal phase track, only the signal at diode CR5 will appear at the output of the combined agc OR gate consisting of diodes CR5, CR6, and CR7.

(6) At times when the phase comparator servo is not nulled, the phase displacement of the 1-kc second IF signal with respect to the corrected 1-kc reference signal at agc detector Q7 would reduce the agc voltage at C8 as a function of that phase difference. In fact, if a 90° shift were encountered, the agc voltage at C8 would tend toward zero, even though there were no actual change in vlf signal level. If this were allowed to occur, the agc-actuated servo cutout (A17) would disable the servo, and phase shifter action would stop. However, a maximum servo detector error voltage would exist at this time because of the large phase displacement. Since the error signal is capacitively coupled to inverter amplifier Q5, a significant signal would appear at OR gate input diode CR6. Consequently, a normal agc signal level would be obtained at the output of the OR gate, and the phase comparator servo would continue to seek a null.

(7) In the event a still larger IF to reference signal shift were encountered by the servo detector, e.g., 180°, a negative voltage would accumulate at agc integrator capacitor C8. In this case a normal agc would be obtained because the integrated signal is applied to unity gain amplifier Q8, where the signal is reversed in phase and is applied to OR gate input diode CR6.

*l. 1-kc IF Amplifier (A16).* A schematic drawing for the 1-kc IF amplifier is shown in figure 3-22. The module contains two separate sections of IF amplification.

(1) The first section is composed of a tuned amplifier and a complementary emitter

follower that accents the output of normal mode second mixer A4 and provides the signal amplification to drive audio amplifier A19.

(2) The second section is composed of tuned amplifier Q4, emitter follower Q5, complementary emitter follower Q6 and Q7, a diode clipper network, an untuned amplifier Q8, emitter follower Q9, and output complementary emitter follower Q10 and Q11. The input to the second section is either the output of normal mode second mixer A4 or the output of 1-kc IF amplifier A3, which follows the X4 second mixer. The output of the second section is used only for the agc and servo phase detectors.

(3) The tuned circuit L2, C8, and C10 in the collector circuit of Q4 is tuned to 1 kc and has a nominal bandpass of 50 cps at the 3-db points. The 50-cps bandpass provides the desired selectivity and ensures the rejection of noise and undesirable harmonics.

(4) The extremely high input impedance of emitter follower Q5 is needed to prevent any significant loading of the tuned circuit in the collector of Q4. The complementary emitter follower (Q6 and Q7) provides the drive current required for the symmetrical clipper (CR1 and CR2). With the additional gain obtained by means of the untuned amplifier (Q8), an overall signal voltage gain of 32 db is achieved. Isolation of the untuned amplifier and restoration of appropriate power levels are accomplished with the unity gain amplifier, which consists of an emitter follower (Q9) and a complementary emitter follower (Q10 and Q11).

*m. Servo Cutout (A17).* The schematic drawing for the servo cutout (A17) is shown in figure 3-23. The module contains the circuits needed to accomplish the following: disable the servo when the carrier level falls to a point too low for reliable phase tracking, control a visual indication of loss of the local frequency standard input, provided appropriate voltages for manual slewing of the servo, and supply a junction point for six selectable panel meter test points.

(1) The local standard input is connected to pin 30(j), through coupling network C1 and R18, and to the detector and filter network consisting of CR1, CR2, C2, and R2. The rectified and filtered local frequency standard input at the base of Q2 causes it to conduct and energize relay K1 when the INTERRUPT WARNING switch is operated. When relay K1 is energized, contacts 4 and 6 and contacts 5 and 3 are closed. K1 is maintained in an energized state by the application of +12 volts through holding contacts 6 and 4. If the local frequency standard output is interrupted, transistor Q2 stops conducting and relay K1 is deenergized. When K1 is deenergized, contacts 6 and 8, and contacts 3 and 1 are closed. With contacts 3 and 1 closed, the PWR STD warning lamp will operate until the local frequency standard output is restored and the INTERRUPT WARNING switch is depressed.

(2) The servo cutout circuit consists of Q1, Q3, relay K2, and associated components. The agc voltage from the agc amplifier (A2) is connected to pin 6(F), through integrator R8 and C3, to the base of Q1. With no carrier present, the voltage at the base of Q1 is approximately +8 volts, which is sufficient to maintain Q1 at cutoff because the emitter of Q1 is biased nominally at +6 volts through network R12, R17, CR3, and R11 from the +12 volt supply. The bias level is adjusted by R17 and establishes the agc threshhold level. With carrier present, the agc level at the base of Q1 drops below the positive threshhold level at the emitter and allows Q1 to conduct. When Q1 conducts, the collector is slightly positive and causes Q3 to conduct and to energize relay K2. With K2 energized, contacts 6 and 8 open and the power from the carrier indicator lamp is removed. At the same time, contacts 5 and 3 are closed, coupling the output of servo driver amplifier (A18) to the servo motor to allow normal tracking. When the carrier is lost or falls below the agc threshhold, Q1 will cease to conduct, causing the collector to go negative and to cut off Q3, thus deenergizing relay K2. With contacts 3 and 5 open, the servo motor is decoupled from the servo driver amplifier and is connected through contact 1 to R13. The path through R13 provides the dynamic braking needed to prevent unwanted coasting

or overshoot. Since contacts 6 and 8 are closed at this time, power is applied to the carrier indicators. Unlike the PWR STD indicator, the carrier indicator extinguishes automatically when the carrier returns.

(3) To prevent the servo from being cut out during momentary interruptions in the carrier, R8 and C3, having a long time constant, hold the level at the base of Q1 high for approximately 15 seconds, but allow cut-out of the servo when vlf transmission ceases for a longer period.

*n. Audio Amplifier (A19).* The schematic drawing for the audio amplifier is shown in figure 3–24. The 1-kc input from the IF amplifier is connected to pin 1(A) and the base of Q1. Transistor Q1 is a driver stage for the subsequent push-pull output stage. It is transformer-coupled to the bases of transistors Q2 and Q3, which are connected in a conventional push-pull arrangement, with audio output transformer T2. The secondary of T2 supplies the driving power for the speaker on the front panel. Resistor R6 and capacitors C5 and C6 make up a tone filter for the aural output. Resistor R3 and diode CR1 provide bias for the push-pull stage, while bias for voltage amplifier Q1 is provided by R1 and R2. Resistor R2 is bypassed by capacitor C1 so that degenerative feedback is provided only by the voltage drop across R1.

*o. Plus and Minus 12-volt Power Supply (A20).* The schematic drawing for the plus and minus 12-volt power supply module is shown in figure 3–25. This module contains the regulator sections of two identical power supplies that furnish the positive and negative 12 volts dc required for the various vlf-12B circuits.

(1) Regulation to within 0.05 percent of the nominal output voltage is provided for line-voltage variations of 95 to 130 volts ac and load variations of 0 to 800 milliamperes. Temperature compensation circuits regulate to within 0.005 percent per degree centigrade. The output ripple is approximately 1 mv peak-to-peak at full load.

(2) Power transformer T1, filter capacitors C1 through C4, transistors Q1 through Q4, and resistors R3 and R4 are mounted on the vlf-12B chassis (see figure 3–8). Transformer T1 has two separate 40-volt rms center-tapped secondary windings. One of these is connected to diodes CR1, CR2, CR3, and CR4 on assembly A20 and the other to diodes CR10, CR11, CR12, and CR13 to make up two separate full-wave rectifiers. One rectifier supplies approximately +56 volts peak to filter input capacitor C4, and the other supplies –28 volts peak to filter input capacitor C3. Regulation of the +12 volts is provided by chassis-mounted series regulator transistors Q4 and Q3. These transistors are controlled by the regulator driver amplifier (Q1), an emitter follower that receives an input signal from the error-detector amplifier.

(3) The following discussion contains references to the circuit module shown in figure 3–25. Transistors Q4 and Q5 comprise a differential amplifier that senses the dc output variations. The network consisting of R13, R14, and R15 (a potentiometer) constitutes a voltage divider across the output, and the center tap of R15 is used to adjust the signal input level to the differential amplifier. Zener diode CR8 is used to establish a reference element for comparison with the output variations. The output of the differential amplifier is applied to dc amplifier Q3, which supplies the driver current for emitter follower Q1, the series regulator driver. Series regulators Q4 and Q3 (on chassis) are connected as a Darlington pair with the emitter of Q3 driving the base of Q4 directly. The Darlington arrangement provides a high dc gain.

(4) Transistor Q2 is used in a current-limiting circuit that protects the series regulators (Q3 and Q4) from accidental shorts or extreme overload by limiting the regular drive signal at the output of emitter follower Q1. To examine the regulating circuit, assume that the output dc tends to increase. The voltage at the base of Q5 will increase a small amount. However, the voltage at the base of Q4 will increase in direct proportion to the output, owing to the action of the Zener diode. This in turn increases the current through Q4 and collector load resistor R12. The increased current through Q4 increases the voltage at the

collector of Q5, which is connected to the base of Q3. This in turn increases the current through Q3, decreasing the collector voltage. The decreased voltage at the base of emitter follower Q1 causes the emitter current and the voltage across emitter resistors R4 and R5 to decrease. In turn, the voltage drop across Q4 (on chassis) is increased, and the output voltage is maintained at the normal value of +12 volts.

(5) If the load voltage tends to decrease, the action of the regulator decreases the voltage drop across Q4, increasing the load voltage to +12 volts. The load voltage can be adjusted approximately ±1.5 volts above and below the +12 volt level by means of potentiometer R15.

(6) Current limiting transistor Q2 normally is cut off. When the load current increases above 1 amp, or an accidental short occurs, Q2 begins to conduct since the emitter voltage, which is normally +12 volts, drops below the voltage at its base. This increased current reduces its collector voltage, which in turn reduces the current through Q1. The reduced current in Q1 reduces the current in Q3 and Q4 (on chassis) and causes the resistance of Q4 to increase, thus limiting the load current. In the event of an actual short, Q4 is cut off, thus presenting a high impedance to the load and reducing the load current to a low value.

(7) Voltage-sensing connections are brought out at pins 11 and 13 to enable sensing of the output at a load operated at some remote point from the supply.

*p. Output Buffers (A25).* Refer to the schematic drawing of figure 3–26. This card is designed to supply the maximum number of buffers that can be mounted on the basic card area. Completely independent in operation, each inverter circuit forms a complete buffer between the input and the output so that shorts at the output will not affect the input circuit.

(1) The circuit is unique in that it utilizes a complementary amplifier to provide a bi-directional low output impedance. This is possible since a separate transistor is in saturation for both the high, "1", and the low, "0," output condition. The output is a true 50-ohm impedance capable of feeding a matched coaxial line without degenerating the leading and trailing edges of pulses.

(2) An input signal, at pin D, is coupled to the bases of transistors Q1 and Q2, by resistors R1 and R2, respectively. The complementary transistors, Q1 and Q2, saturate or turn off as the respective bases are driven by the input signal. With a positive logical "1," input signal transistor Q1 turns off and transistor Q2 turns on. Resistors R3 and R4 supply a back bias to the respective transistors, thus giving the circuit high temperature stability. Resistors R5 and R6 are used to supply a minimum output resistance since the saturation resistance of the transistors is approximately 15 ohms. These resistors also form collector loads used to protect the transistors from damage in case the output is inadvertently shorted.

(3) In the event of a very small output current, resistor R7 or R8 maintains a design minimum collector current. This is necessary to avoid problems created by the variation of transistor beta at low-level saturation currents.

*q. 100-kc Amplifier and Phase Shifter (A14).* This circuit is used only in models containing the mechanical servo. (In receivers that contain the electronic servo, this module is replaced by a delay line and phase shifter module in the same card location.) The schematic drawing of the 100-kc amplifier and phase shifter is shown in figure 3–27.

(1) The input from the local frequency standard is coupled through C5 and R25 at pin 5(E) to a symmetrical clipper consisting of CR1 and CR2. The clipped signal is capacitively coupled to emitter follower Q7 to isolate the clipper and to provide driving power to amplifier Q8. The output is connected to pin 2(B). When the 1-mc option is used, pin 2(B) connects to a MOD–10 module, which is used to divide the 1 mc to 100 kc, and to a rear panel switch that is used to select either the 100-kc or 1-mc source. If only a 100-kc input is used, pin 2(B) is jumpered to 10(L), where it is coupled through C8 and R34 to a 100-kc amplifier and filter, Q9.

(2) Transistor Q9 provides some amplification to the 100-kc signal, which is then filtered by low-pass filter C9, C10, and L1. The resulting 100-kc sinewave is coupled to paraphase amplifier Q10, which provides output sinewaves of equal amplitude having a 180° phase relationship to each other. These signals appear at pins 12(N) and 14(R) for connection to the externally mounted phase shifter. An rc network divides the signals into four 90° quadrants.

(3) The phase shifter is in effect a motor-driven capacitor with four segments, one for each quadrant. It changes capacitance and thus shifts the phase of the 100-kc local standard signal in direct proportion to the remaining detected phase error between the local standard signal and the 1-kc second IF. The shifted output, a coherent 100-kc signal, is obtained from pin 5 of the phase shifter and is connected to pin 30(j) of the 100-kc amplifier. From pin 30(j), the coherent 100-kc signal is coupled to emitter follower Q1, which isolates the external phase shifter from amplifier Q2. After being amplified by Q2, the 100-kc signal is coupled to another emitter follower (Q3), which drives a Schmitt trigger (Q4 and Q5). Here the coherent sinewave is squared and is applied, through emitter follower Q6, to a dc restorer (C14 and CR3) to achieve the proper logic level needed to operate elements of the divider chain, and to integrator R24 and C4, which produces a 100-kc monitor signal for the panel meter.

*r. 76.8- to 100-KC Converter Assembly (A24).* This option arrangement enables the direct comparison of a 76.8-kc frequency standard with all of the receivable vlf channels applied at the vlf-12B input.

(1) This option is accomplished by insertion of a special 76.8-kc to 100-kc converter printed-circuit card into connector XA24. When this special card is inserted, the local standard input switch on the rear of the panel can be used to select a 100-kc input or a 76.8-kc input. This option works the same as the 1-mc/100-kc frequency standard input option. The input level required is 0.5 to 15 volts rms. The input impedance is 10,000 ohms or greater. These characteristics are identical to those of the local frequency standard input of the normal vlf-12B.

(2) The conversion from 76.8 kc to 100 kc is accomplished by a series of multiplication and division techniques. The specific process in this case is to multiply by 5, divide by 6, multiply by 5, divide by 4, multiply by 5, and finally divide by 4. This arrangement provides a composite multiplication ratio of 125/96, which converts 76.8 kc to 100 kc. A detailed circuit schematic is shown in figure 3-28. The 76.8-kc input is supplied from A14 (100-kc amplifier and phase shifter). The circuits contained on A14 will amplify and clamp the frequency standard signal so that the input to the 76.8-kc to 100-kc converter is squared and has an amplitude of approximately 6 volts peak to peak. This signal is applied to the X5 multiplier consisting of the Q1, Q2, and Q3 circuits. Q1 is the basic multiplier and has a resonant circuit tuned to 384 kc. The fifth harmonic is selected by the tuned circuit and applied to the input of Q2. Q2 and Q3 constitute a squaring and buffer circuit which ensures that the output waveform of the X5 multiplier is of adequate amplitude and rise time to properly operate the digital divider circuit that follows.

(3) The divide-by-6 circuit is made up of FF1, FF2, FF3, and utilizes integrated circuits. In this case Fairchild flat-pack DT$\mu$L integrated logic circuits are used. The logic connection is a basic binary divider which incorporates feedback to accomplish the divide-by-6 function. The feedback provides a divide-by-3 and then a divide-by-2 logic, thus producing a square-wave output. This square-wave output is an optimum waveform for the following X5 multiplier.

(4) The X5 multiplier, represented by the Q4, Q5, and Q6 circuits, is almost identical to the X5 multiplier previously described. The only difference is that the resonant circuit is tuned to 320 kc, thus selecting the fifth harmonic of the input frequency.

(5) The divide-by-4 circuit, represented by FF4 and FF5, utilizes the same Fairchild flat-packs previously mentioned. In this case,

however, the logic is a standard binary divider without feedback. The resonant circuit of the last X5 multiplier is tuned to 40 kc, the fifth harmonic of its input frequency. The output of the last divide-by-4 circuit is a 100-kc square wave, which is phase-coherent with the 76.8 kc input.

*s. Servo Motor Driver (A18).* Figure 3–29 is a schematic diagram for this module. The servo motor driver module is used only in receivers containing the mechanical servo. The input from the servo phase detector is connected to pin 7(H). At this point the ±dc error signal is chopped at a nominal 1-kc rate by chopper transistor Q1, which is operated by a 1-kc astable multivibrator (Q7 and Q10). Chopping of the error signal provides an ac error signal which can be capacitively coupled to the amplifiers. This eliminates the need for dc amplifiers and their inherent drift problems. The chopped 1-kc signal is capacitively coupled to emitter follower Q2. The output of this emitter follower provides drive to amplifier Q3. Capacitor C4, in the collector circuit of Q3, is used to remove any spikes which may occur as a result of the chopping. The output of Q3 is coupled to another emitter follower, Q4, whose output is capacitively coupled to complementary emitter follower Q5 and Q6. The output from this circuit, taken from the emitters, is coupled to a synchronous demodulator through transformer T1, which provides complementary inputs of the error signal to the two bi-directional transistors, Q11 and Q12. Complementary 1-kc square-wave inputs from the 1-kc astable multivibrator are fed to the base circuits, to provide reference signals for the synchronous demodulator. When the phase of the signal from the servo phase detector advances relative to the reference, a positive dc is provided at the output of the demodulator; conversely, a negative dc is provided when the phase is retarded. This ±dc error is coupled to complementary emitter follower Q13 and Q14, which provides driving power to the servo motor at pin 30(j). The output of emitter follower Q2 is also coupled to the agc phase detector, through integrator R37 and C15, to help provide synchronous agc.

## 3–9. Power Control and Protective Circuits

Refer to the schematic given in figure 3–8 for the power control and protective circuits of the vlf-12B (115-volt ac operation). Primary power of 95 to 130 volts ac, 48 to 40 cps, is supplied through two lines to 3-pin connector J1 at the rear of the vlf-12B; the third line is used for chassis grounding. The connector is an integral part of line filter FL1, which is used to reduce radiofrequency interference (rfi) transmitted by power lines. A shielded twisted-pair from the filter is connected through a lighted pushbutton switch, S9, on the front panel and a 0.5-ampere slow-blow fuse, F1, located on the rear panel, to the primary winding of power transformer T1. The lighted switch (S9) provides a visual indication of uninterrupted power.

## 3–10. Plus 24–Volt DC Operation (Optional)

*a.* In a vlf-12B provided with this option, a dc-to-dc converter is used for obtaining standby power automatically from an external 24-volt dc battery supply in the event of ac power failure. The schematic drawing of the converter is shown in figure 3–30. Twenty-four volts dc ±1 volt is connected to terminal strip TB1 located on the rear panel of the vlf-12B. (See figure 3–8.)

*b.* The completely sealed converter unit contains a dc-to-ac inverter, which supplies current to the primary of a power transformer that has three separate secondary windings. Rectifiers for each winding are contained in the same unit. The unit furnishes two 36-volt, two 18-volt, and one 9-volt dc output. Externally, the 36-volt outputs are connected to separate 12-volt dc regulators.

*c.* A transfer to battery source power is accomplished when the primary ac line voltage drops below 90 volts. When this happens, the effective reverse bias, normally applied to the converter rectifier diodes by the vlf-12B power supply, is reduced and the battery source supplies the required current. The transfer is accomplished without interruption of power.

*d.* A battery supply capable of providing 24 volts dc ±1 volt for a minimum period of 8 hours is recommended. This implies the use of batteries having a rating of at least 7.8 ampere-hours.

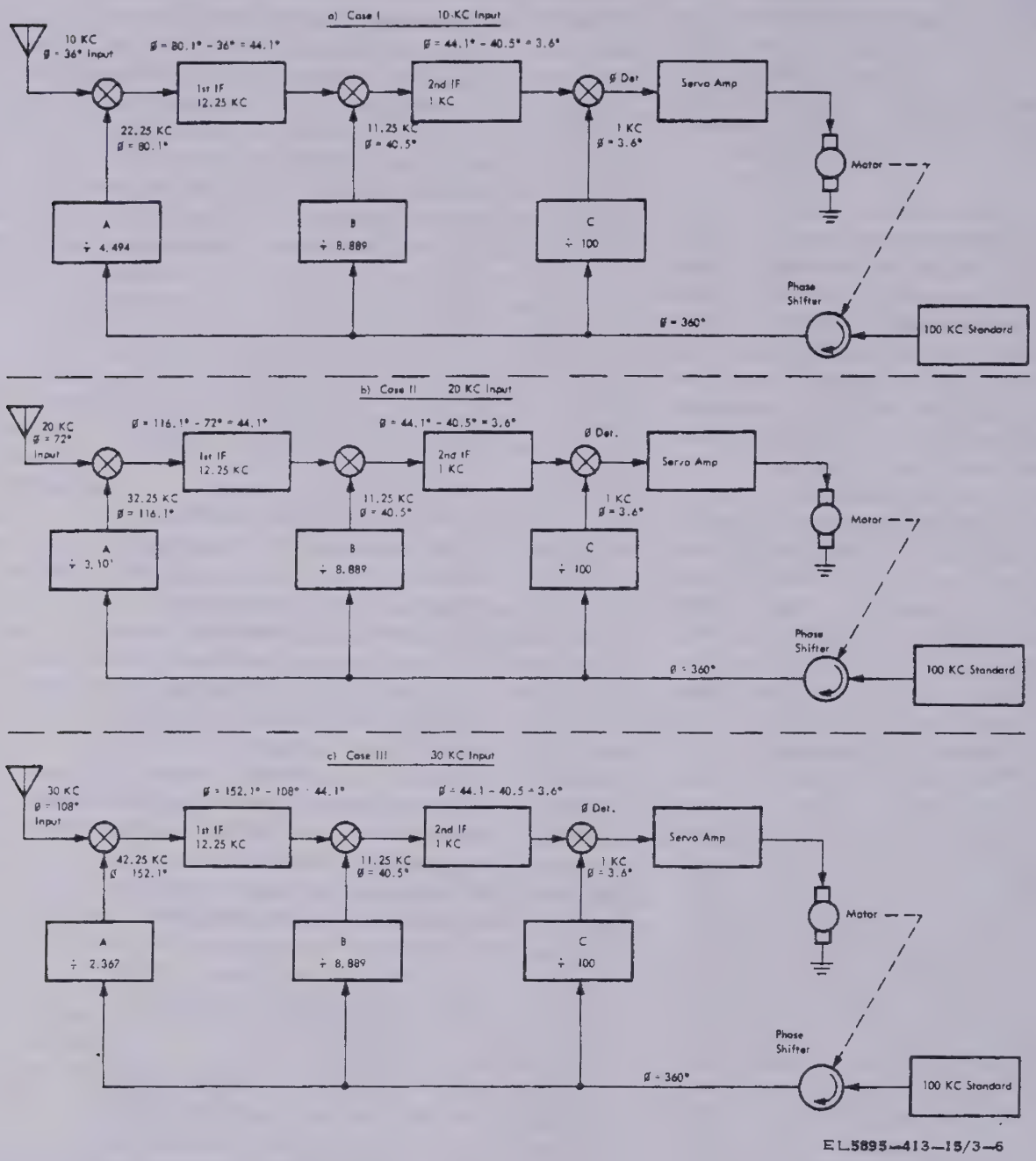



*Figure 3–1. Functional diagram of basic vlf–12B receiver-phase comparator*

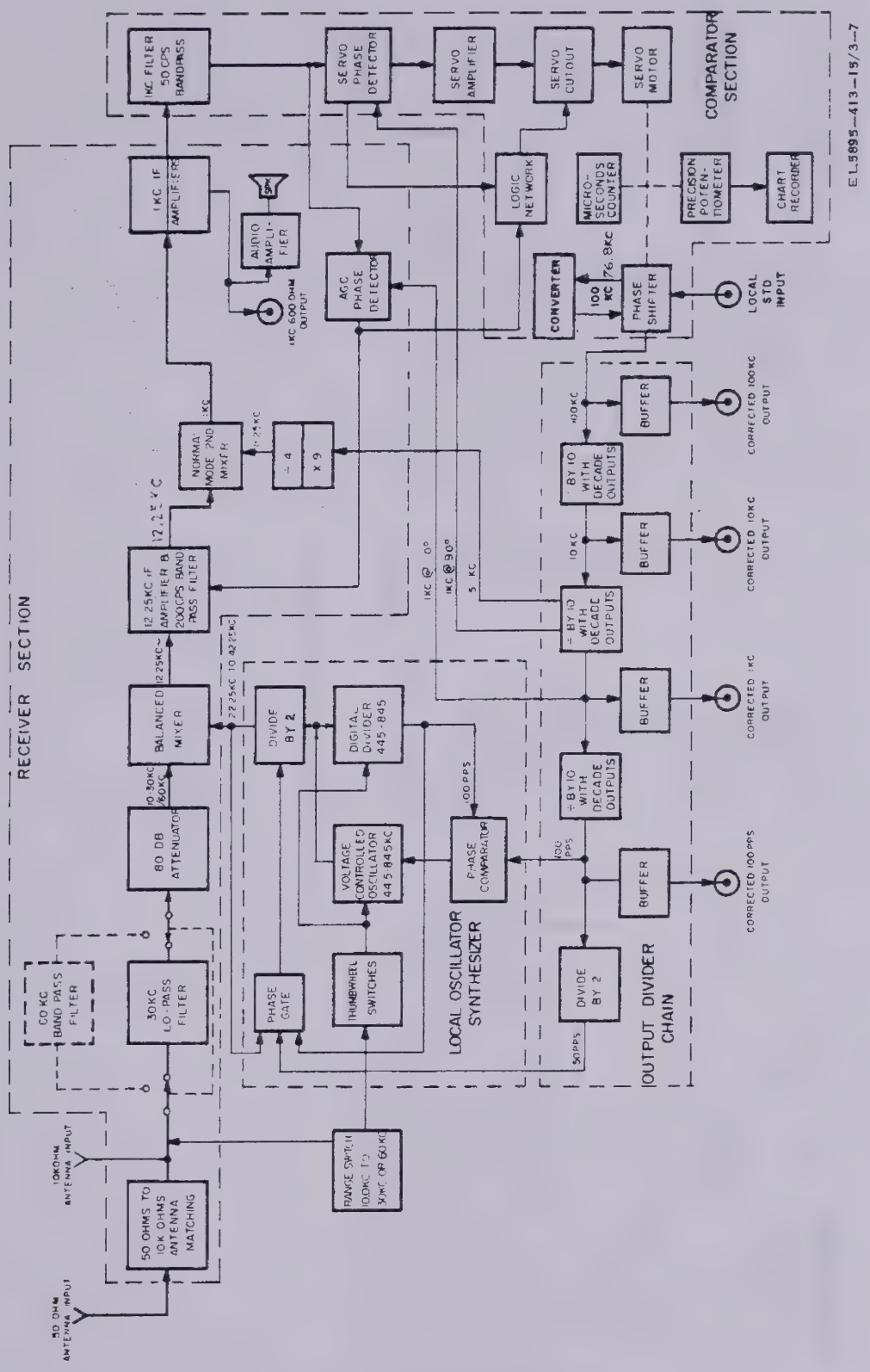



*Figure 3-2. Simplified block diagram, vlf-12B receiver-phase comparator*

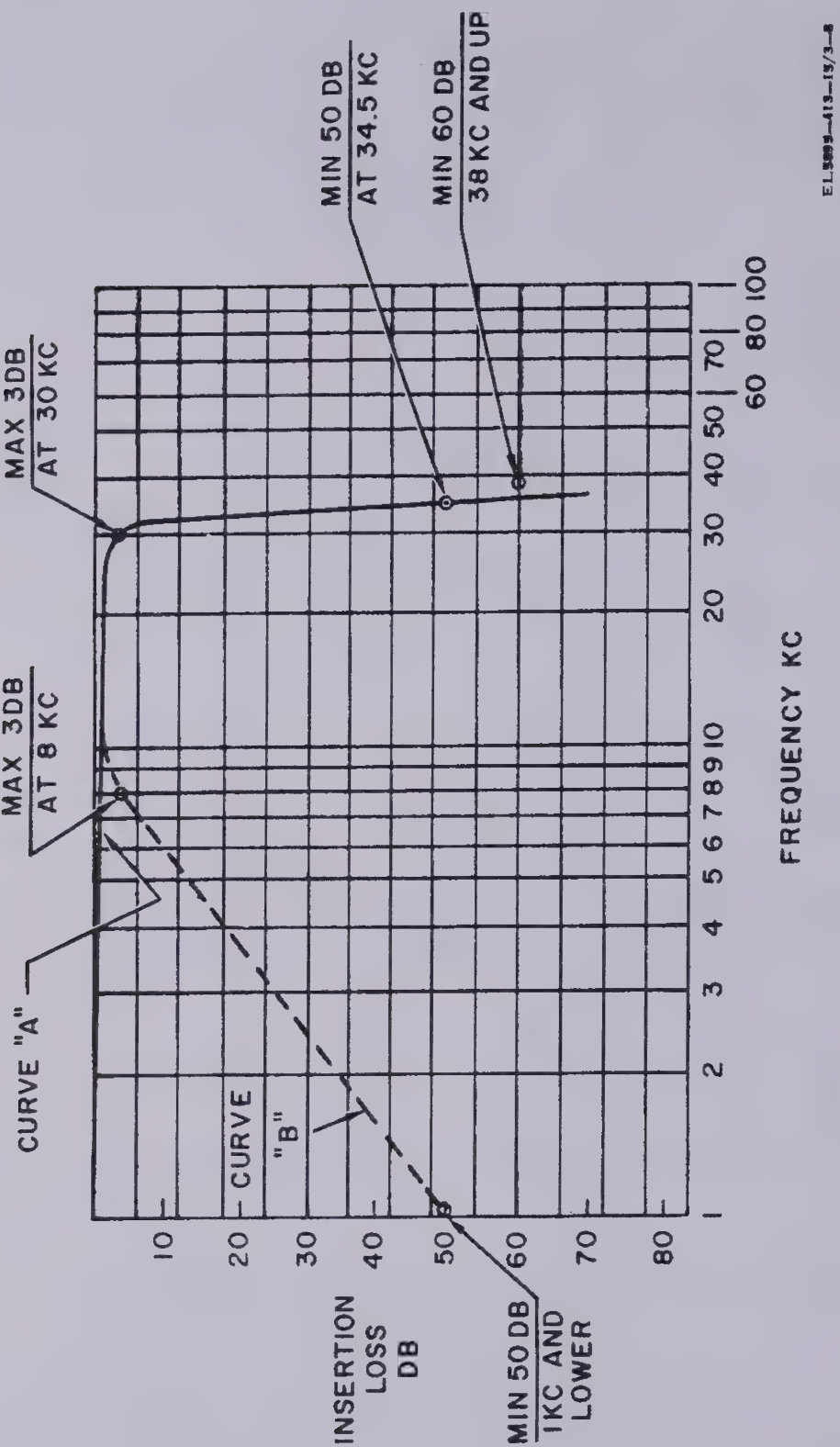



*Figure 3-3. Response curve for 30-kc low-pass filter*

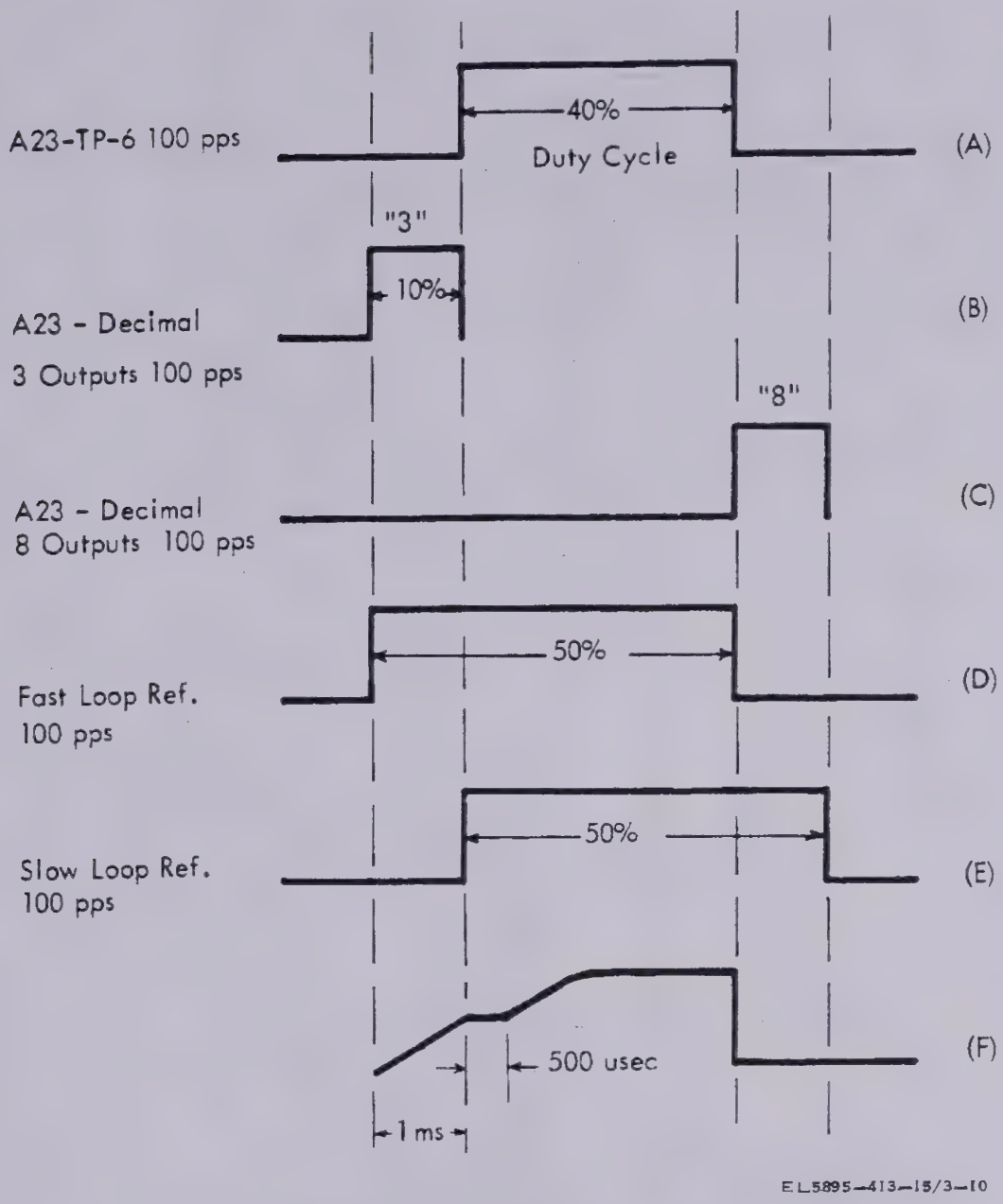



*Figure 3-5. Phase detector waveforms*

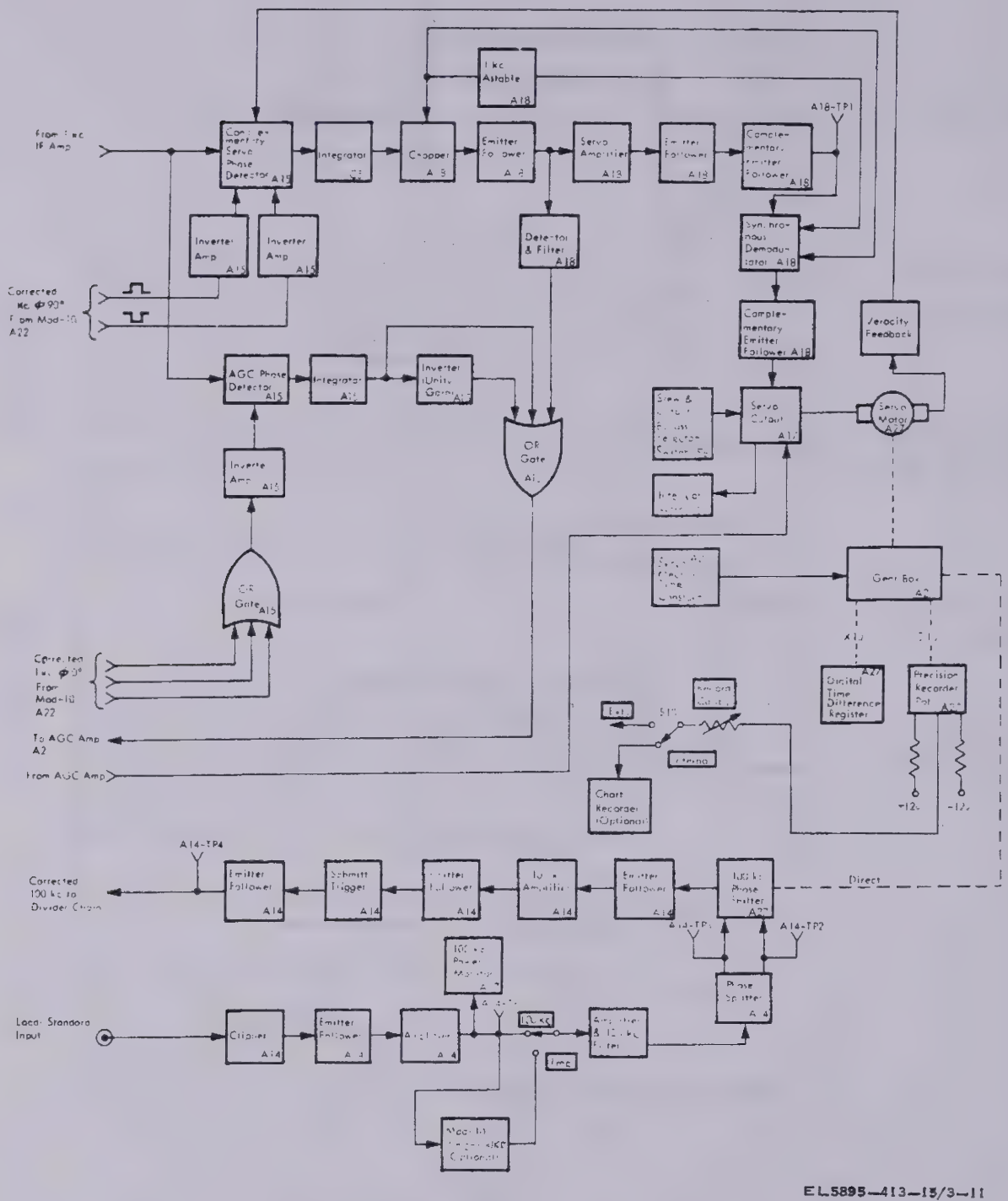



*Figure 3-6. Detailed block diagram, mechanical servo*

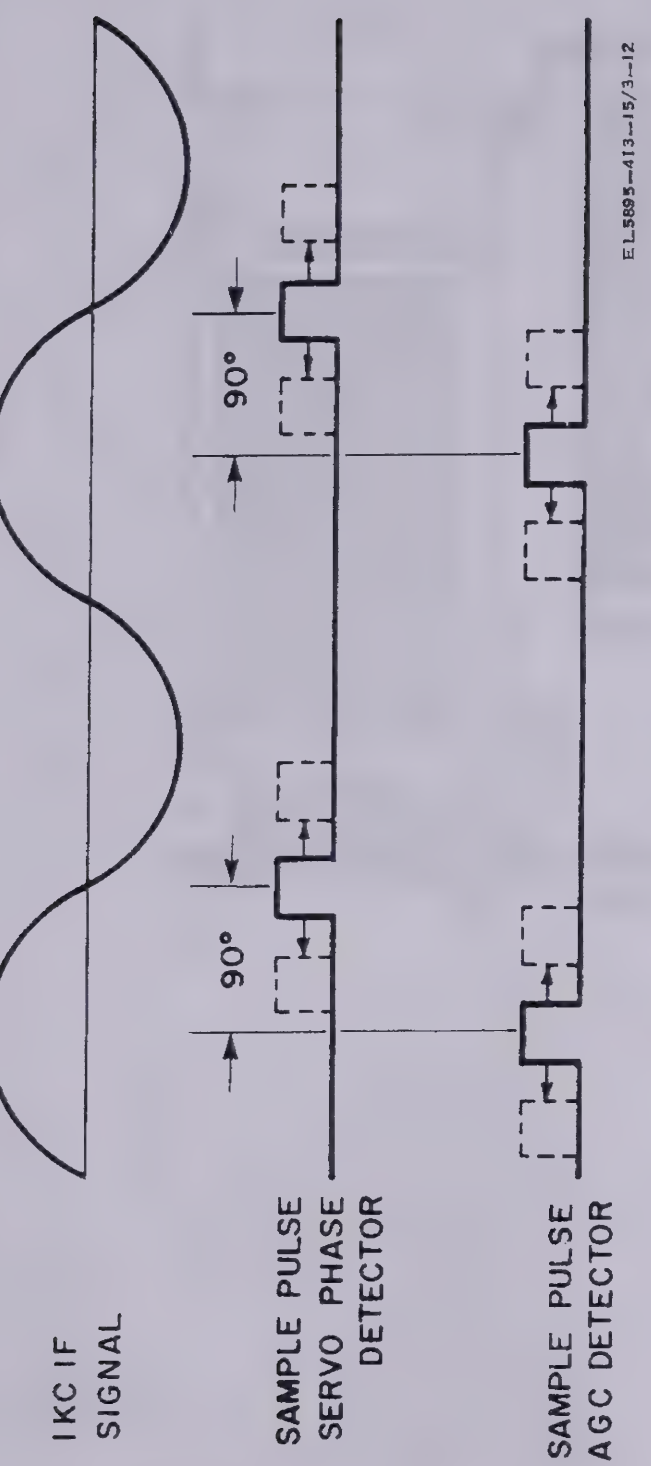
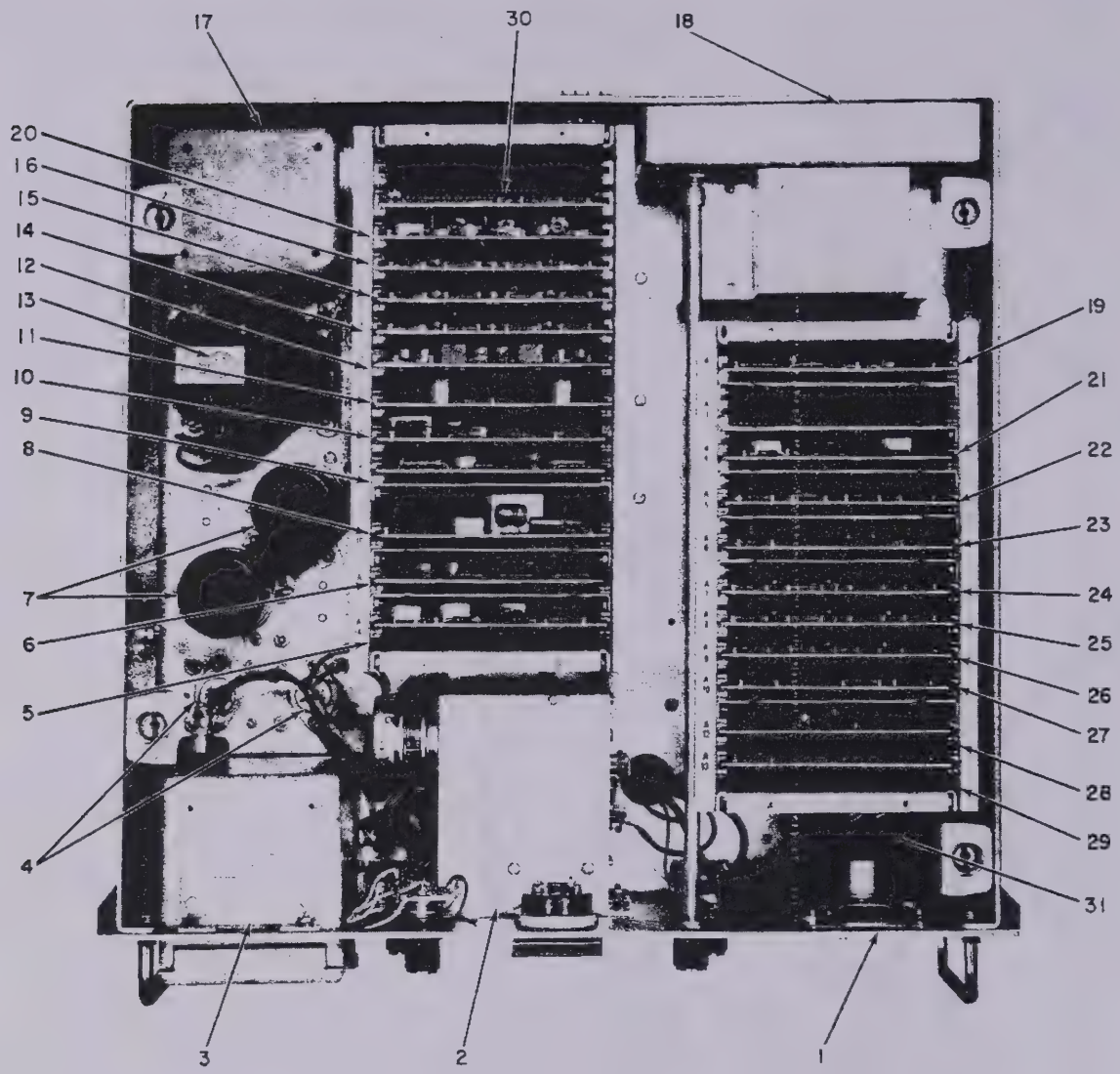

1 2 3 4 5 6 7 8 9 10 1 2 3 4 5 6 7 8 9 0
IKC IF SIGNAL
90°
90°
SAMPLE PULSE SERVO PHASE DETECTOR
SAMPLE PULSE AGC DETECTOR
EL5895-413-15/3-12

*Figure 3-7. Sampling technique of phase detectors*




1. SPEAKER
2. A27 - SERVO ASSY
3. CHART RECORDER
4. Q2 & Q4 - DC POWER SUPPLY REG TSTR
5. A14 - 100-KC AMPLIFIER AND PHASE SHIFTER
6. A15 - SERVO & AGC PHASE DETECTOR
7. $C_1$ & $C_2$ - POWER SUPPLY CAPACITORS
8. A16 - 1-KC IF. AMPLIFIER
9. A17 - SERVO CUTOUT
10. A18 - SERVO MOTOR DRIVER
11. A19 - AUDIO AMPLIFIER
12. A20 - ± 12-VOLT POWER SUPPLY
13. T1 - POWER SUPPLY TRANSFORMER
14. A21 MOD-10 - 100-KC TO 10-KC DIVIDER
15. A22 MOD-10 - 10-KC TO 1-KC DIVIDER
16. A23 MOD 10 - 1-KC to 100-PPS DIVIDER
17. DC-TO-DC CONVERTER
18. A1 - RF MODULE
19. A2 - 12.25-KC IF. AMPLIFIER
20. A24 - 76.8 TO 100-KC CONVERTER
21. A4 - NORMAL MODE 2ND MIXER
22. A5 - 3 FLIP-FLOPS & GATES
23. A6 - VCO AND LOCAL OSCILLATOR
24. A7 - MOD-10 UNITS DIVIDER
25. A8 - MOD-10 TENS DIVIDER
26. A9 - 4 FLIP-FLOPS
27. A10 - ONE SHOT & RESET
28. A12 - SYNTHESIZER $\phi$ DET (SLOW-LOOP)
29. A13 - SYNTHESIZER $\phi$ DET (FAST-LOOP)
30. A25 - OUTPUT BUFFERS
31. A28 - THUMBWHEEL SWITCH ASSEMBLY

EL5895-413-15/3-14

*Figure 3-9. VLF-12B receiver-phase comparator, top view*

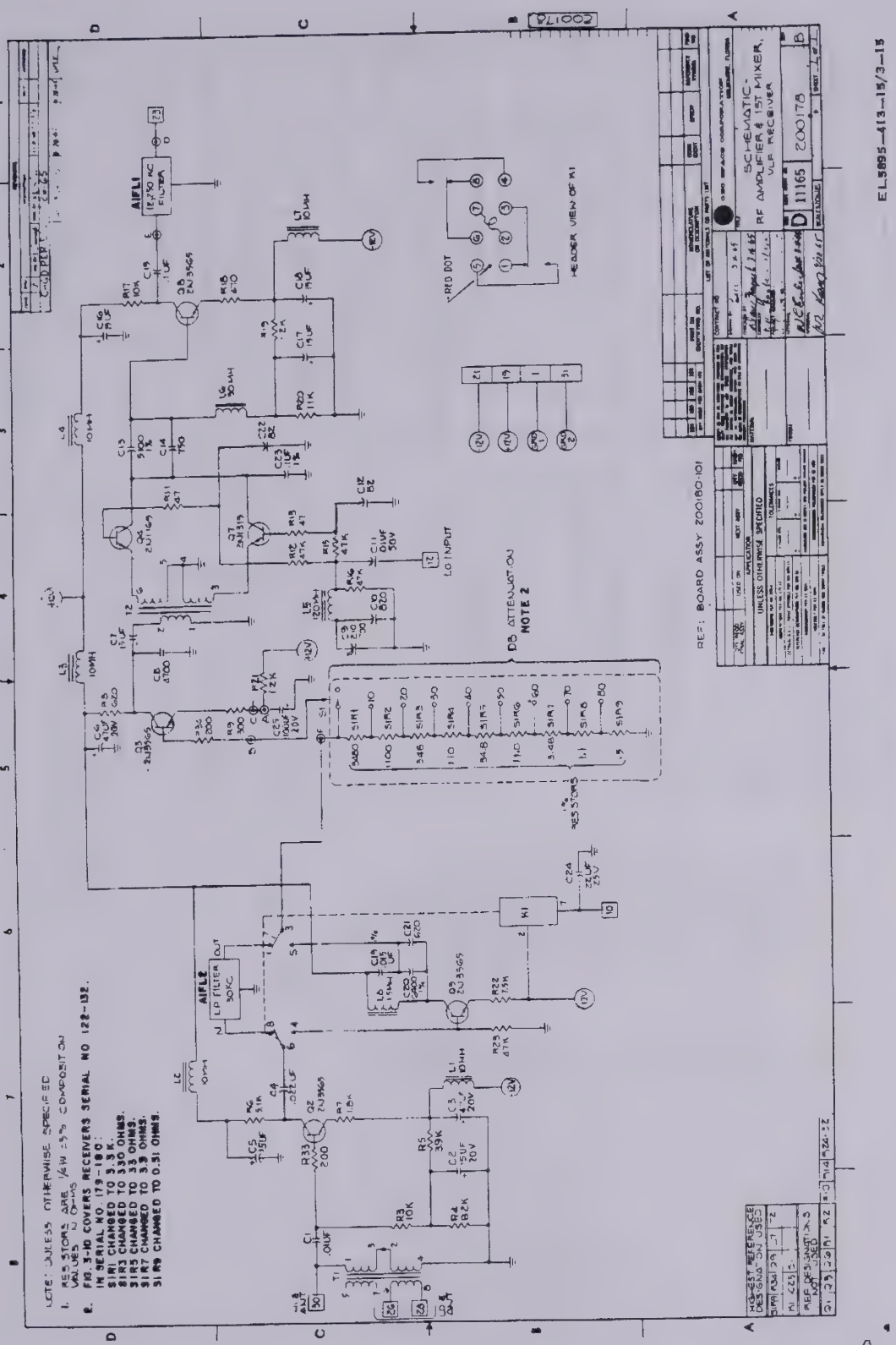
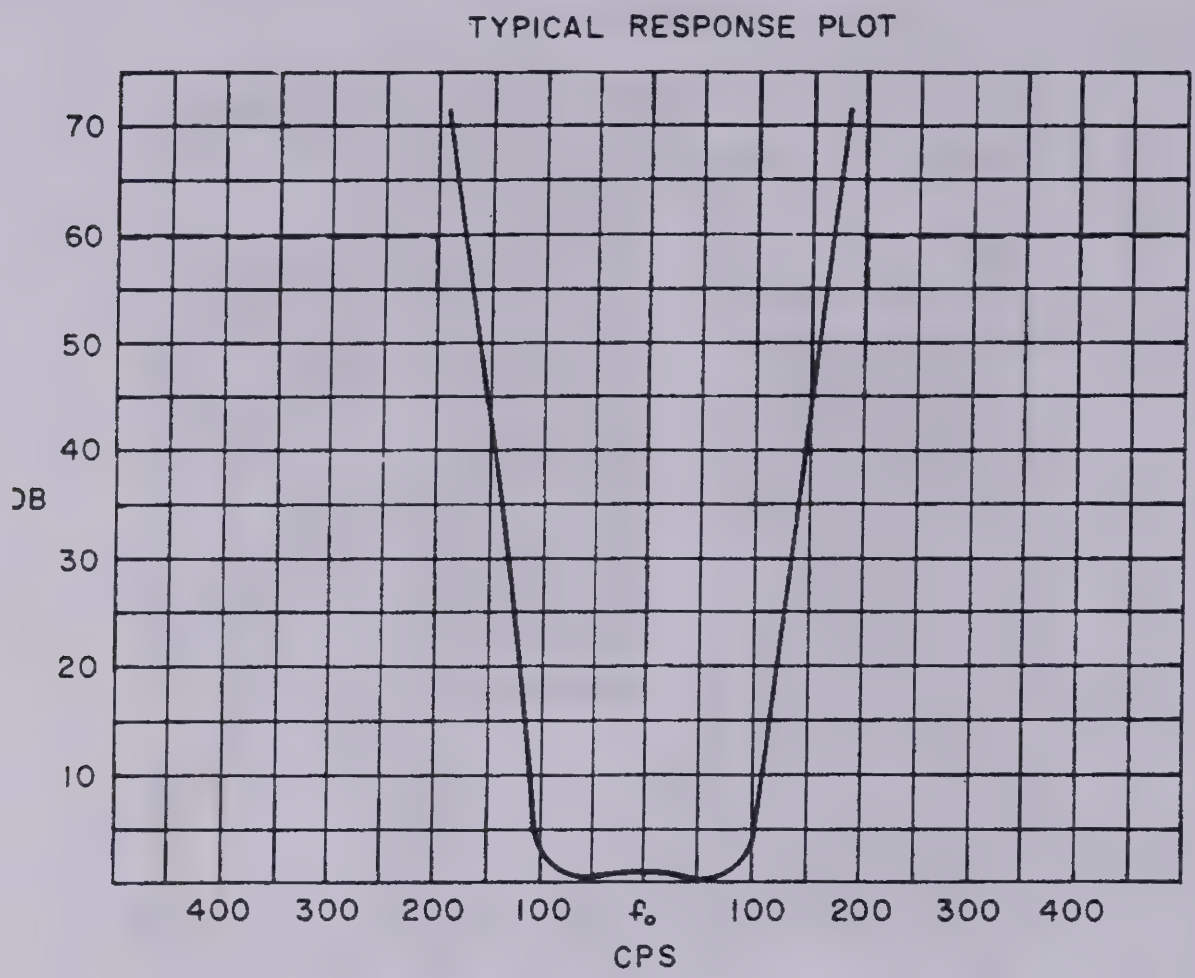



*Figure 3-10. Schematic, RF amplifier and first mixer assembly, A1*

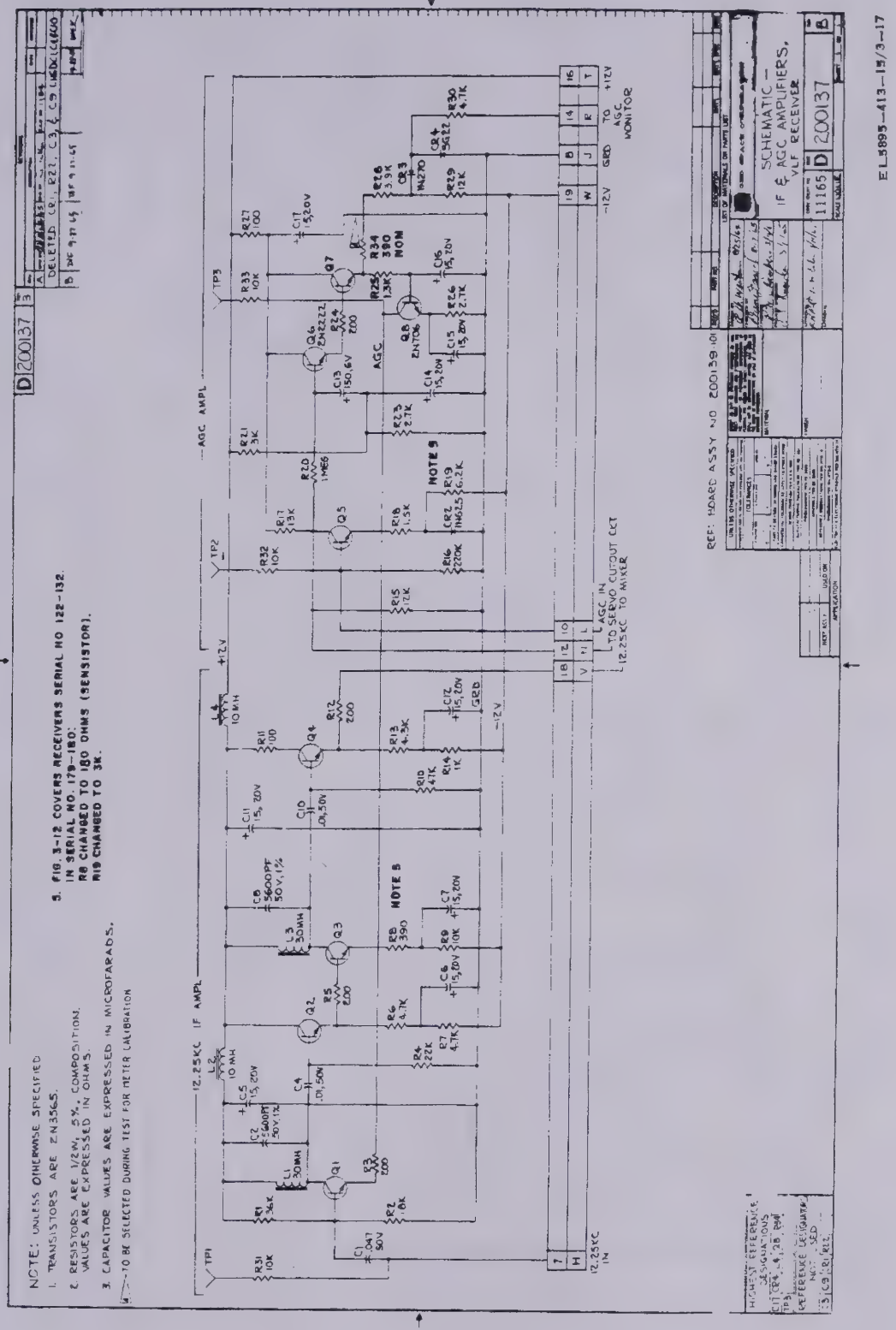



TYPICAL VALUES

| L3 | U3 | L60 | U60 | RIP | I.L |
|---|---|---|---|---|---|
| 101 | 101 | 170 | 174 | .5 | 3.0 |

EL5895-413-15/3-16

*Figure 3-11. Characteristic curve of crystal filter FL1*




EL5895-413-15/3-17

*Figure 3-12. Schematic, 12.25-kc IF and age amplifier assembly, A2*

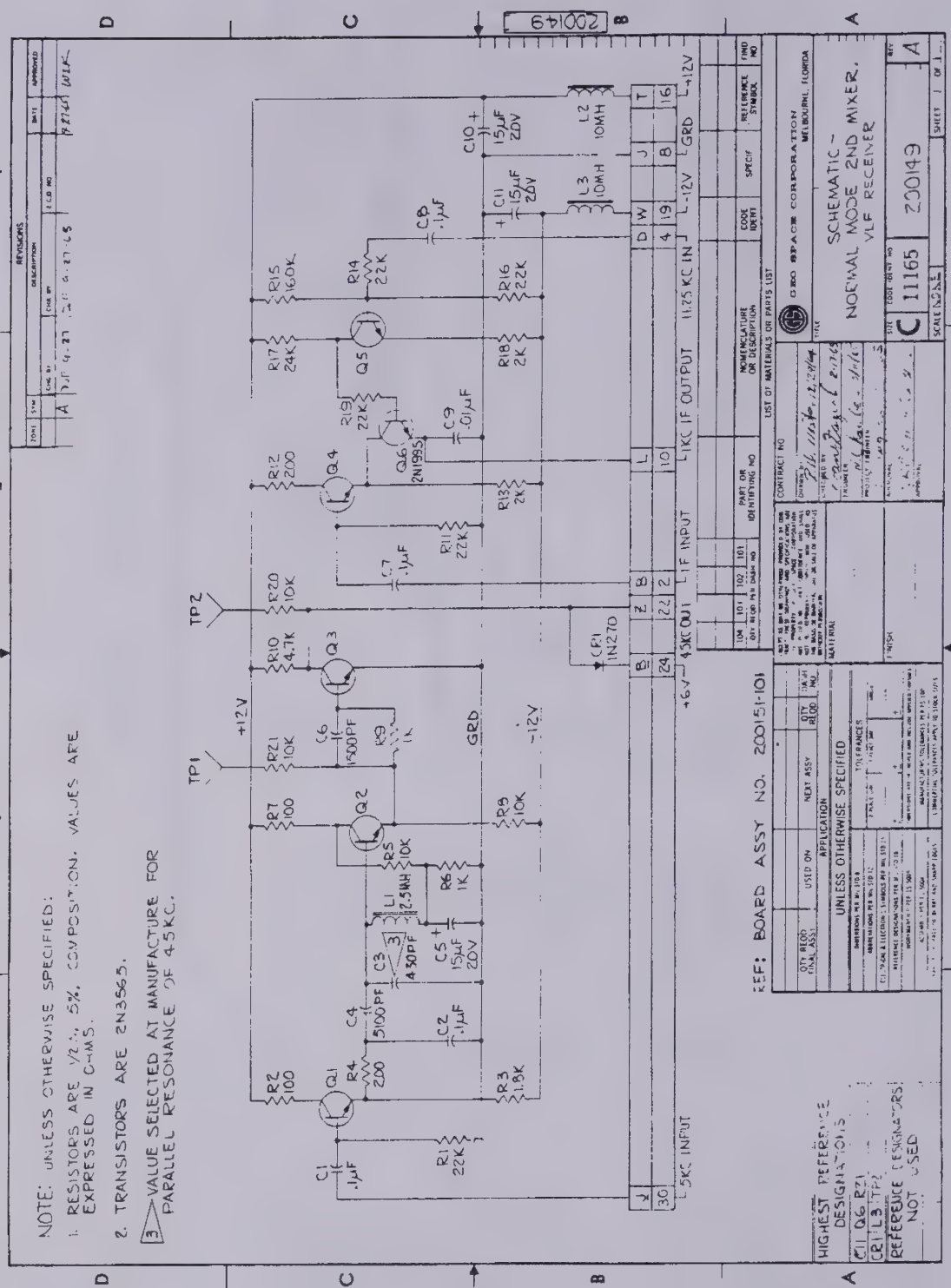



*Figure 3-18. Schematic, second mixer assembly, A4*

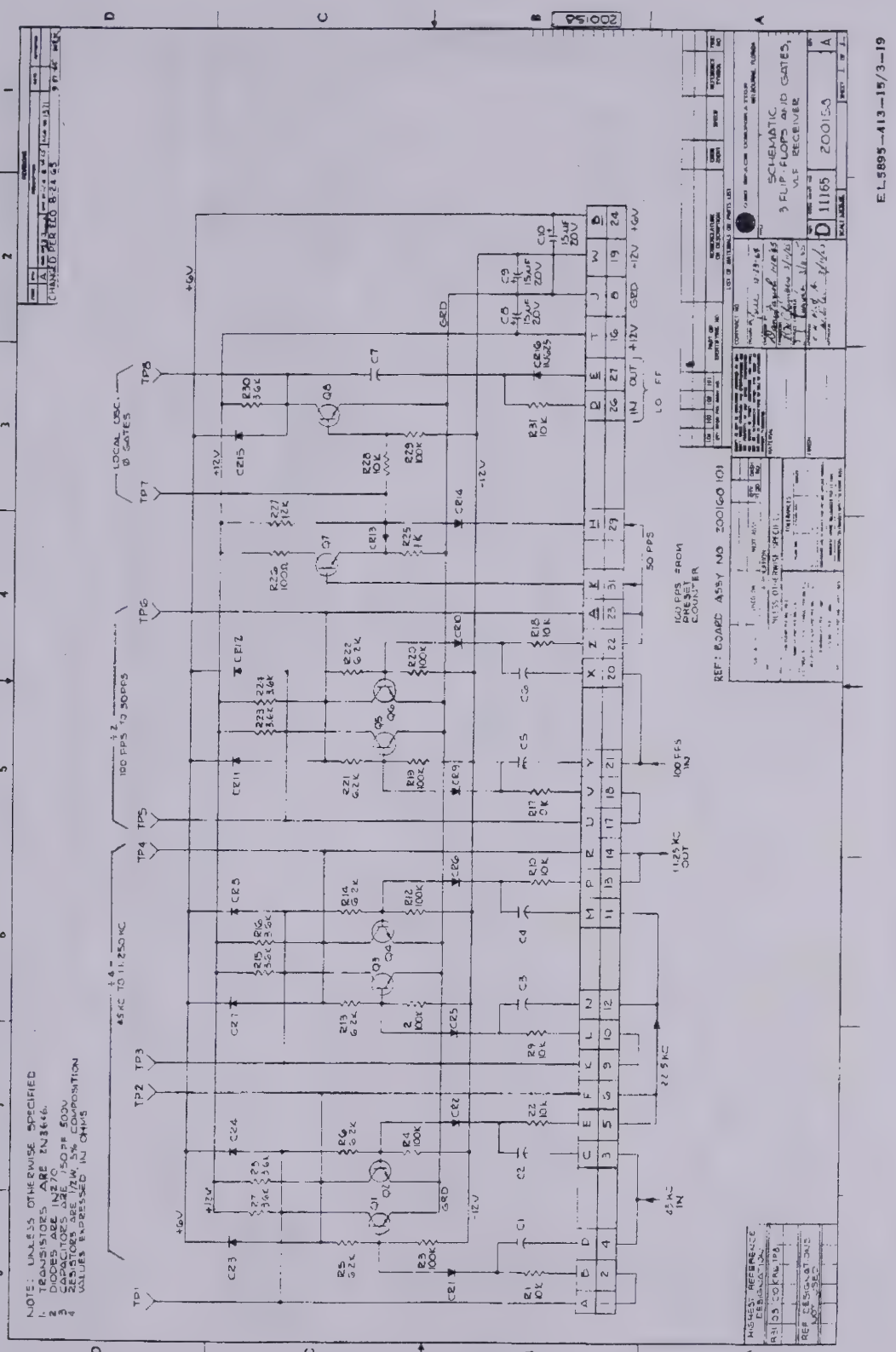



*Figure 3-14. Schematic, three flip-flops and gates assembly, A5*

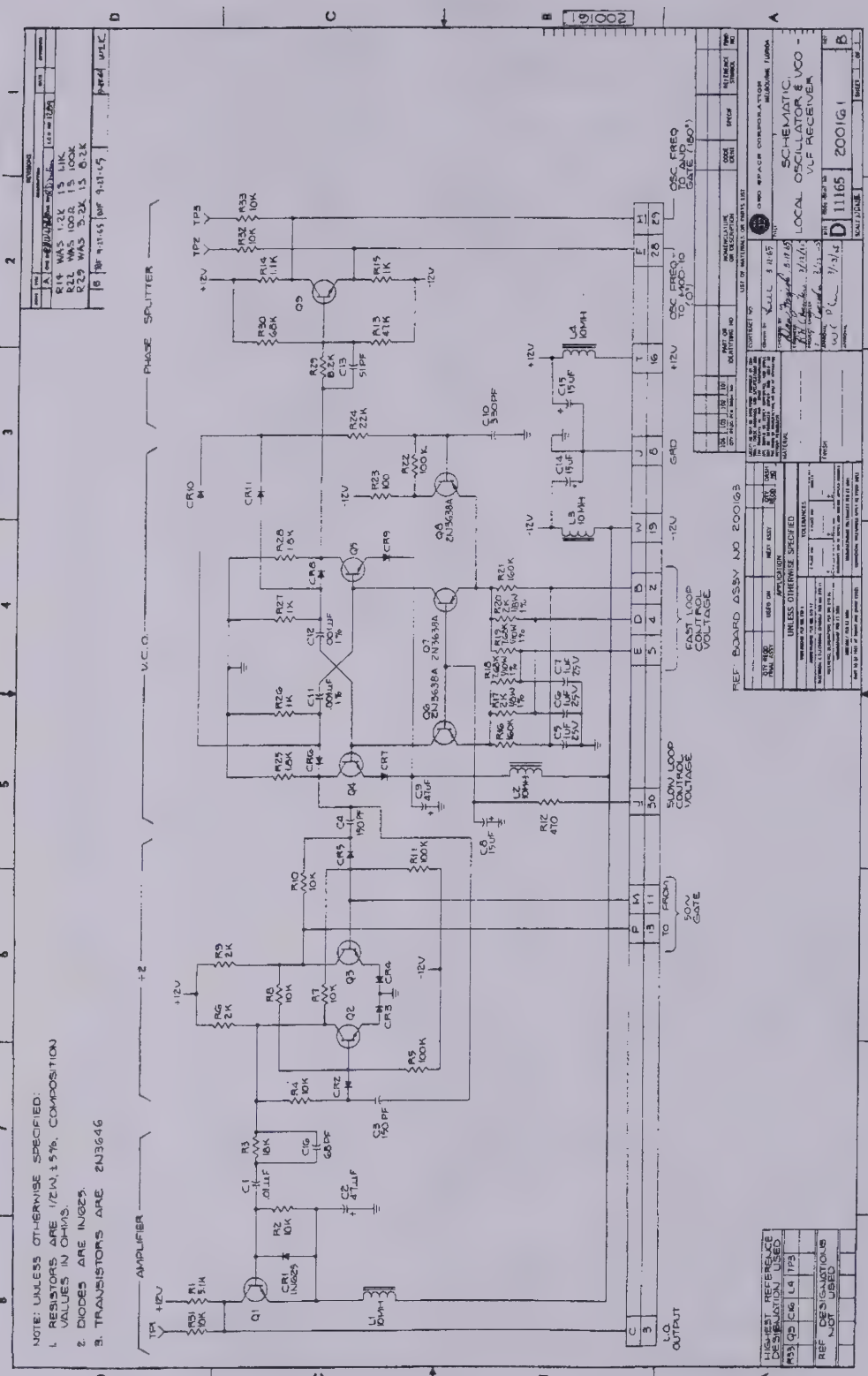
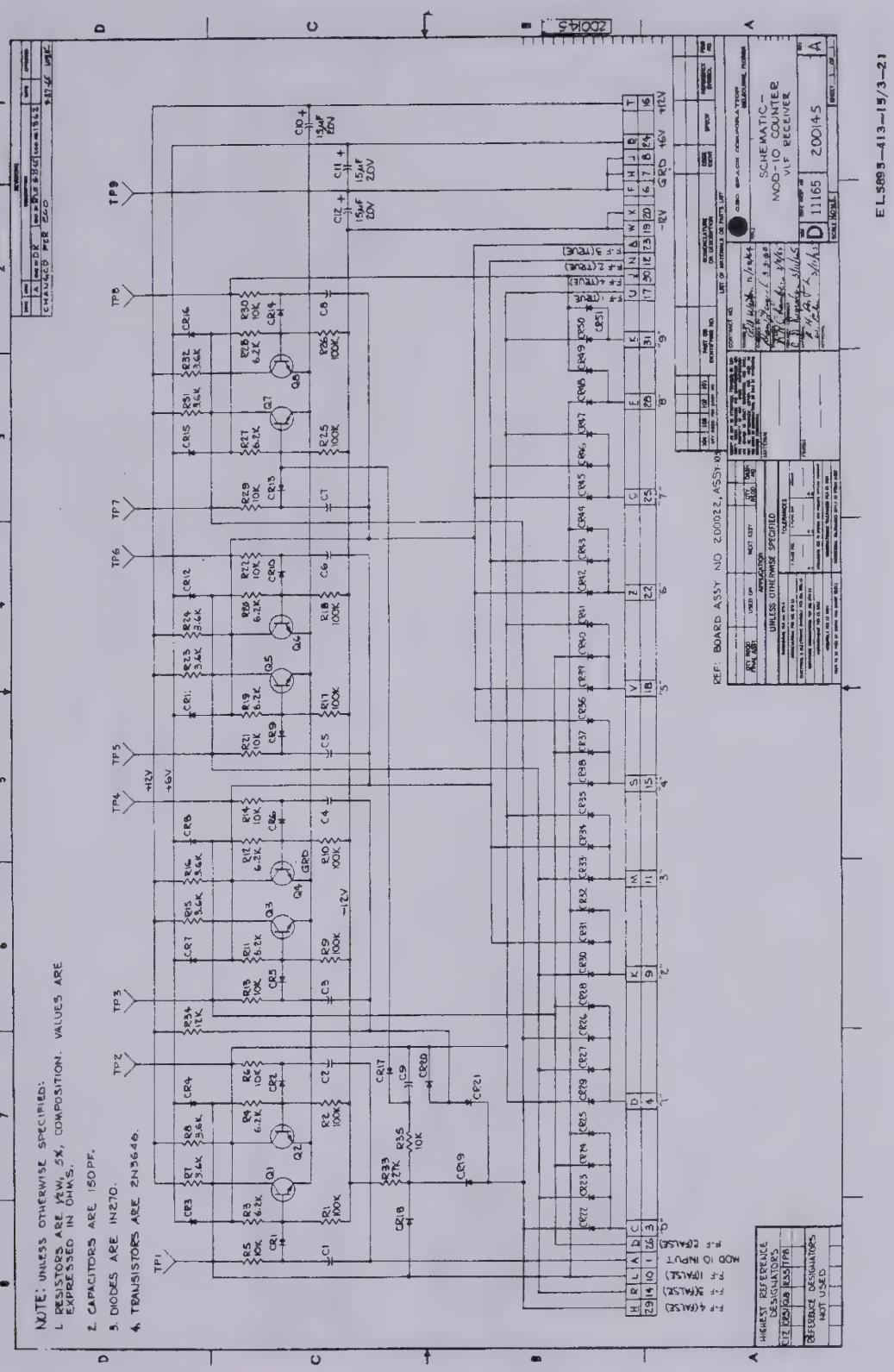



Figure 3-15. Schematic, local oscillator and VCO assembly, A6

*Figure 3-15. Schematic, local oscillator and VCO assembly, A6*




EL 5895-413-15/3-21

*Figure 3-16. Schematic, MOD-10 counter assembly, A7, A8, A21, A22, and A23*

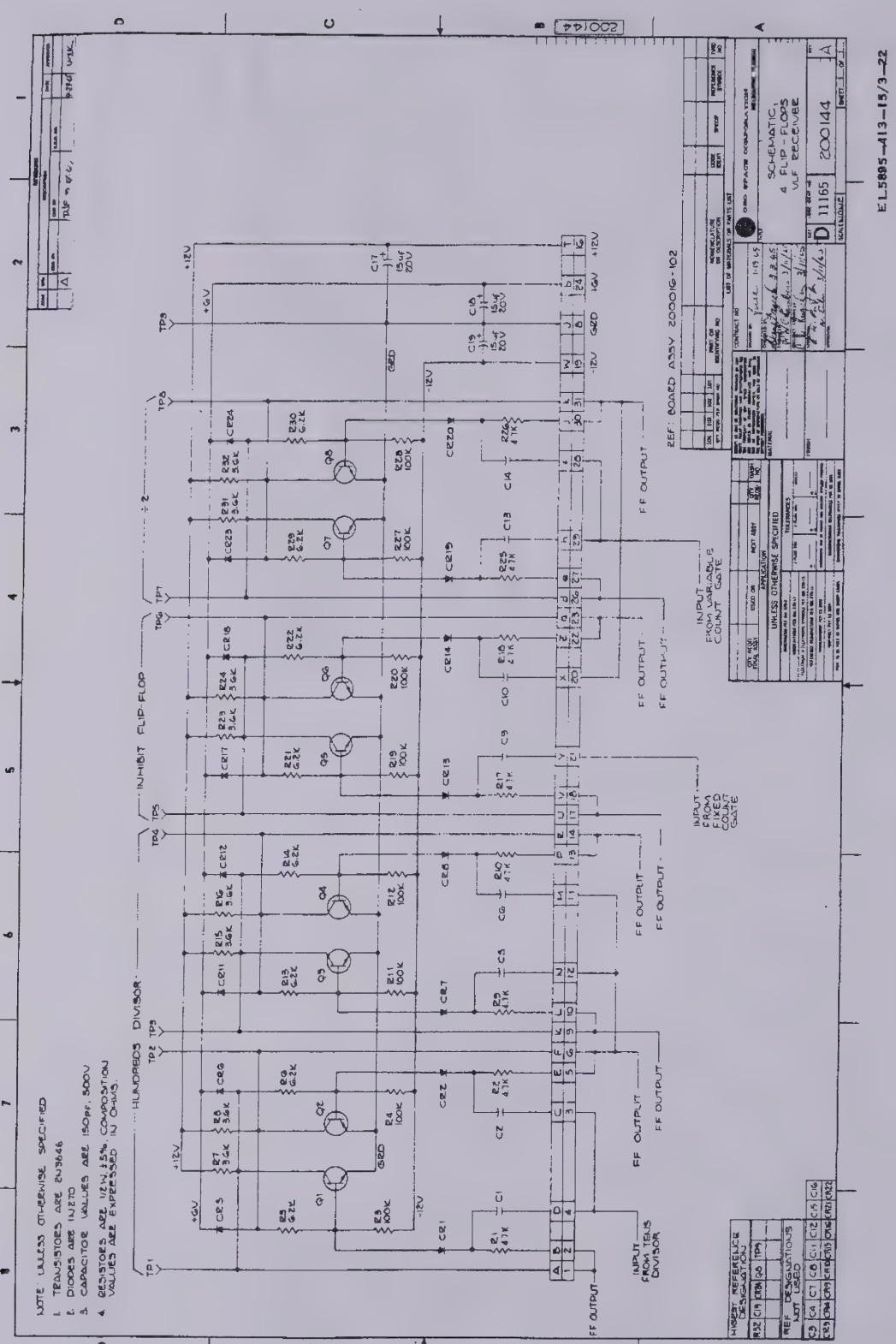



*Figure 3-17. Schematic, four flip-flops assembly, A9*

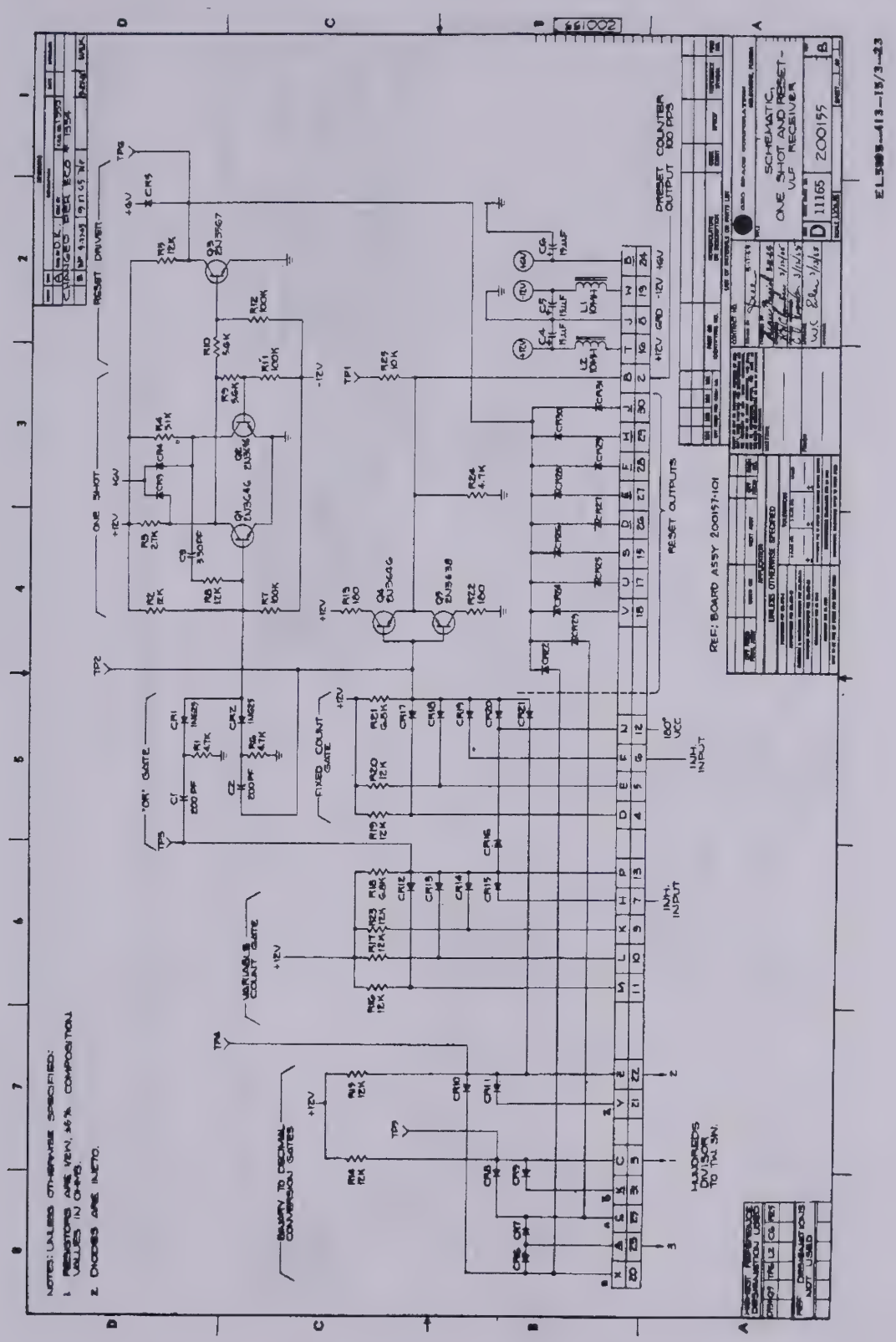

SCHEMATIC, ONE SHOT AND RESET - VLF RECEIVER
D 1165 200155
RESET DRIVER
ONE SHOT
RESET OUTPUTS
PRESET COUNTER OUTPUT 100 PPS
REF: BOARD ASSY 200157-101
NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/8W, ±5% COMPOSITION. VALUES IN OHMS.
2. DIODES ARE IN270.

*Figure 3-18. Schematic, one-shot and reset assembly, A10*

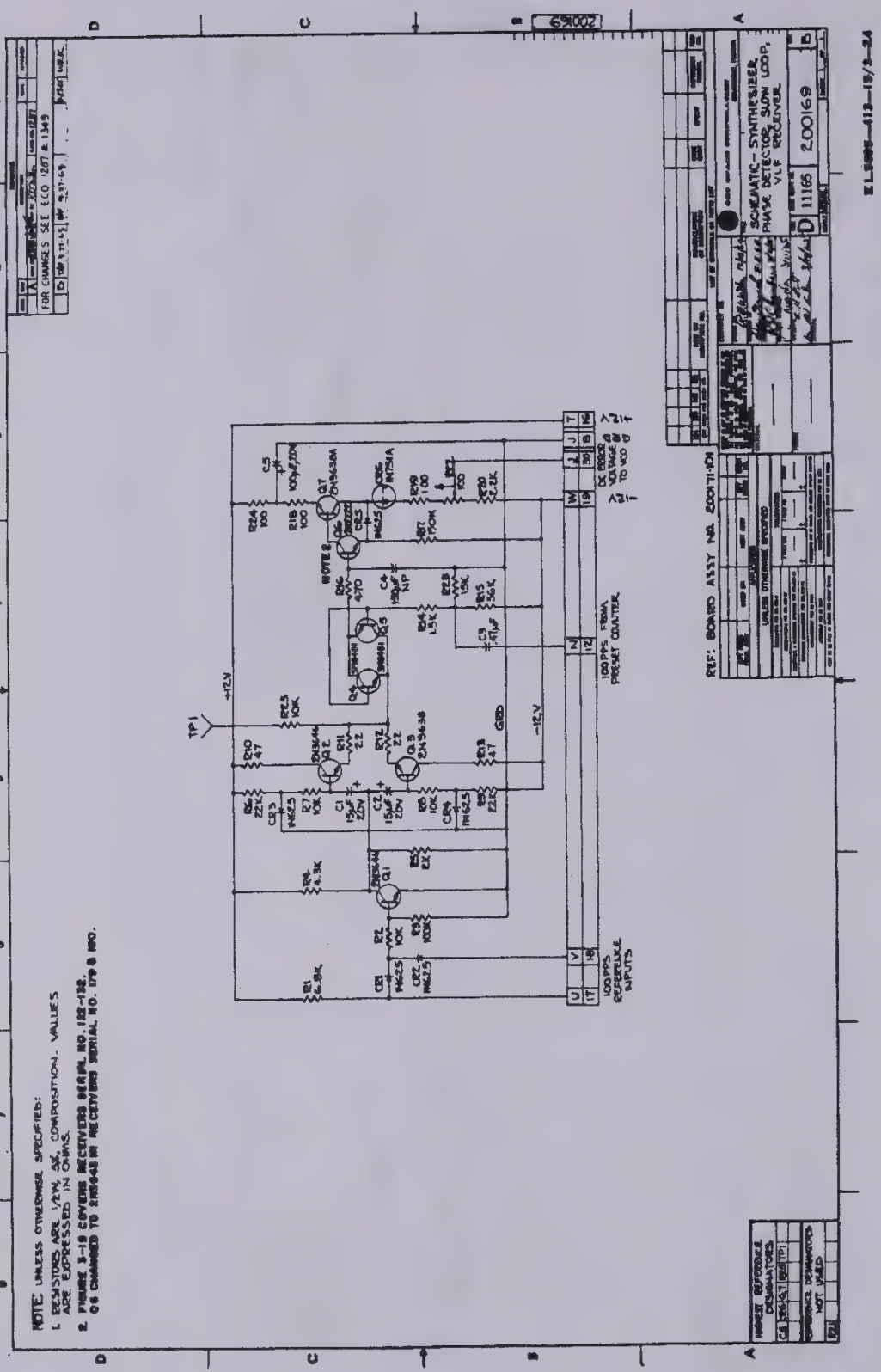



*Figure 3-19. Schematic, synthesizer phase detector (slow-loop) assembly, A12*

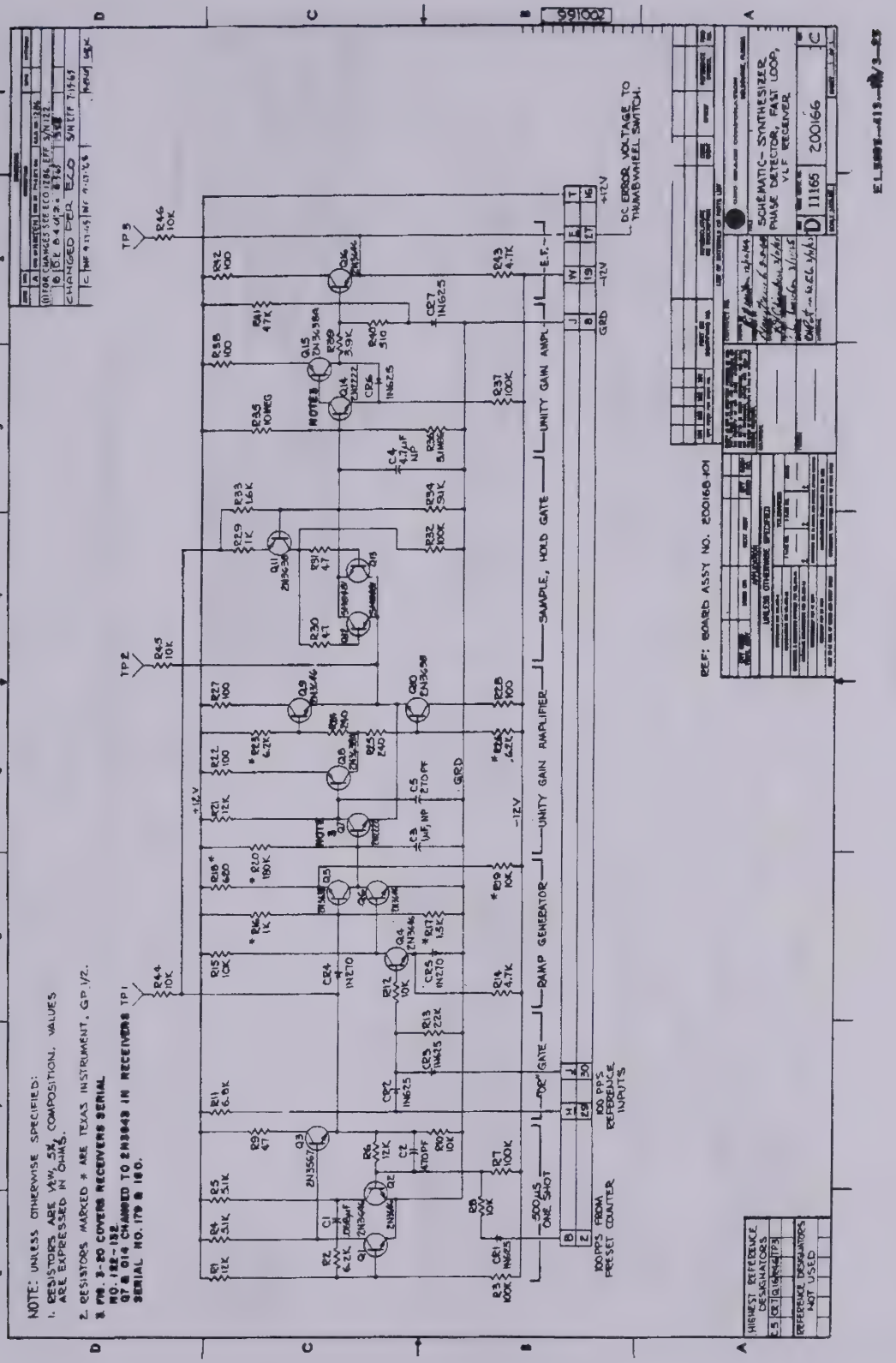

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE ¼W, 5% COMPOSITION. VALUES ARE EXPRESSED IN OHMS.
2. RESISTORS MARKED * ARE TEXAS INSTRUMENT, GP 1/2.
3. FOR 3-20 COVERS RECEIVERS SERIAL NO. 182-135. Q7 & Q14 CHANGED TO 2N3640 IN RECEIVERS SERIAL NO. 179 & 180.
TP1
TP2
TP3
+12V
-12V
GRD
RAMP GENERATOR
UNITY GAIN AMPLIFIER
SAMPLE, HOLD GATE
UNITY GAIN AMPL
500 µS ONE SHOT
100 PPS FROM PRESET COUNTER
100 PPS REFERENCE INPUTS
DC ERROR VOLTAGE TO THUMBWHEEL SWITCH.
REF: BOARD ASSY NO. 200168-101
SCHEMATIC- SYNTHESIZER PHASE DETECTOR, FAST LOOP, VLF RECEIVER
200166
D 11166

*Figure 3-20. Schematic, synthesizer phase detector (fast-loop) assembly, A13*

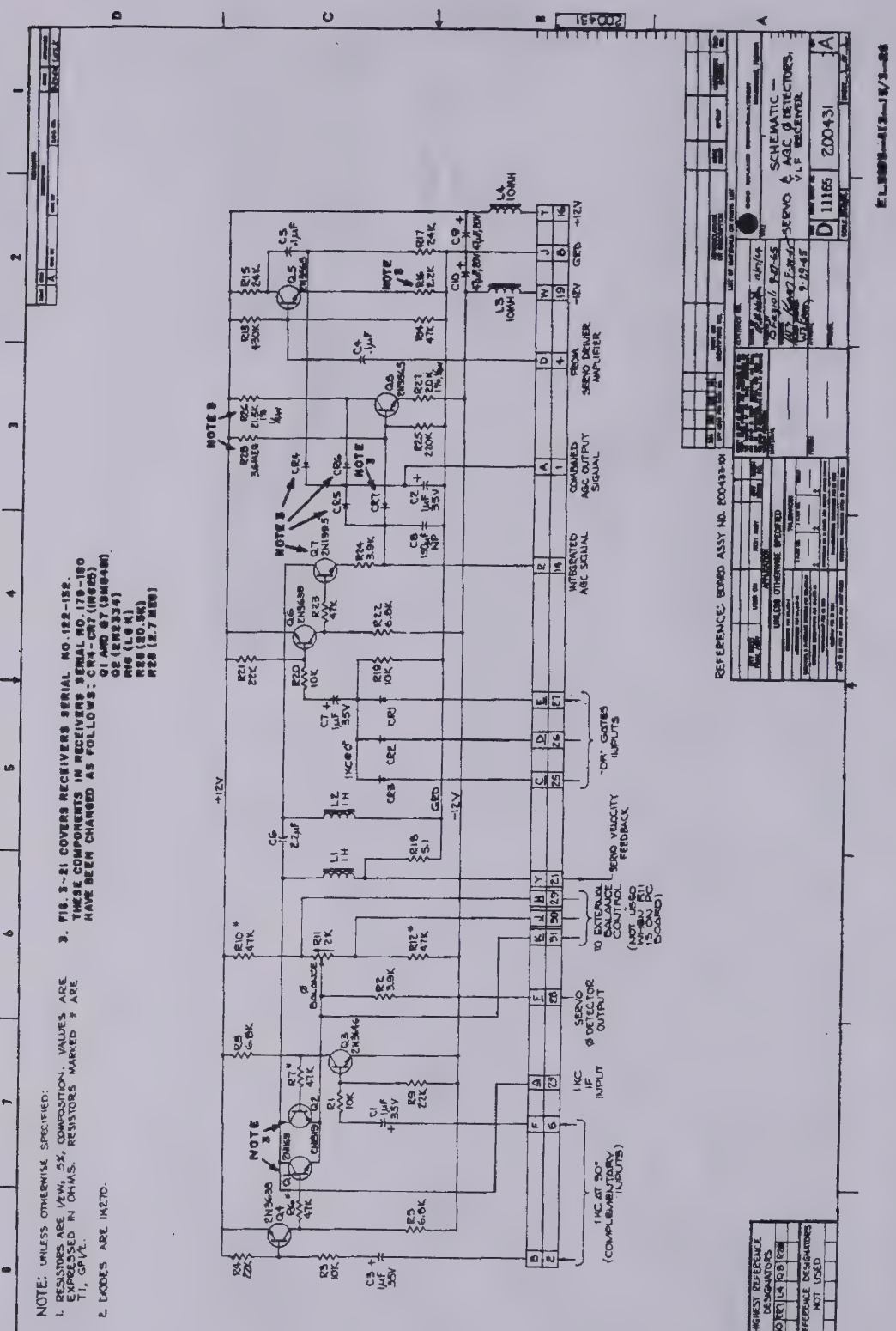

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/4W, 5%, COMPOSITION. VALUES ARE EXPRESSED IN OHMS. RESISTORS MARKED * ARE T1, GPVE.
2. DIODES ARE IN270.
3. FIG. 3-21 COVERS RECEIVERS SERIAL NO. 122-132. THESE COMPONENTS IN RECEIVERS SERIAL NO. 178-180 HAVE BEEN CHANGED AS FOLLOWS: CR14-CR17 (IN645) Q1 AND Q7 (2N1995) Q2 (2N2324) R16 (1.6K) R18 (10.5K) R26 (2.7 MEG)
NOTE 3
+12V
-12V
GND
1KC IF INPUT
1KC 90° (COMPLEMENTARY INPUTS)
SERVO Ø DETECTOR OUTPUT
Ø BALANCE
TO EXTERNAL BALANCE CONTROL
(NOT USED WHEN R11 IS ON PC BOARD)
SERVO VELOCITY FEEDBACK
"OR" GATES INPUTS
INTEGRATED AGC SIGNAL
COMBINED AGC OUTPUT SIGNAL
FROM SERVO DRIVER AMPLIFIER
REFERENCE: BOARD ASSY NO. 200433-101
SCHEMATIC — SERVO & AGC Ø DETECTORS, V.L.F. RECEIVER
D 11165 200431 A

*Figure 3-21. Schematic, servo and agc phase detectors assembly, A15*

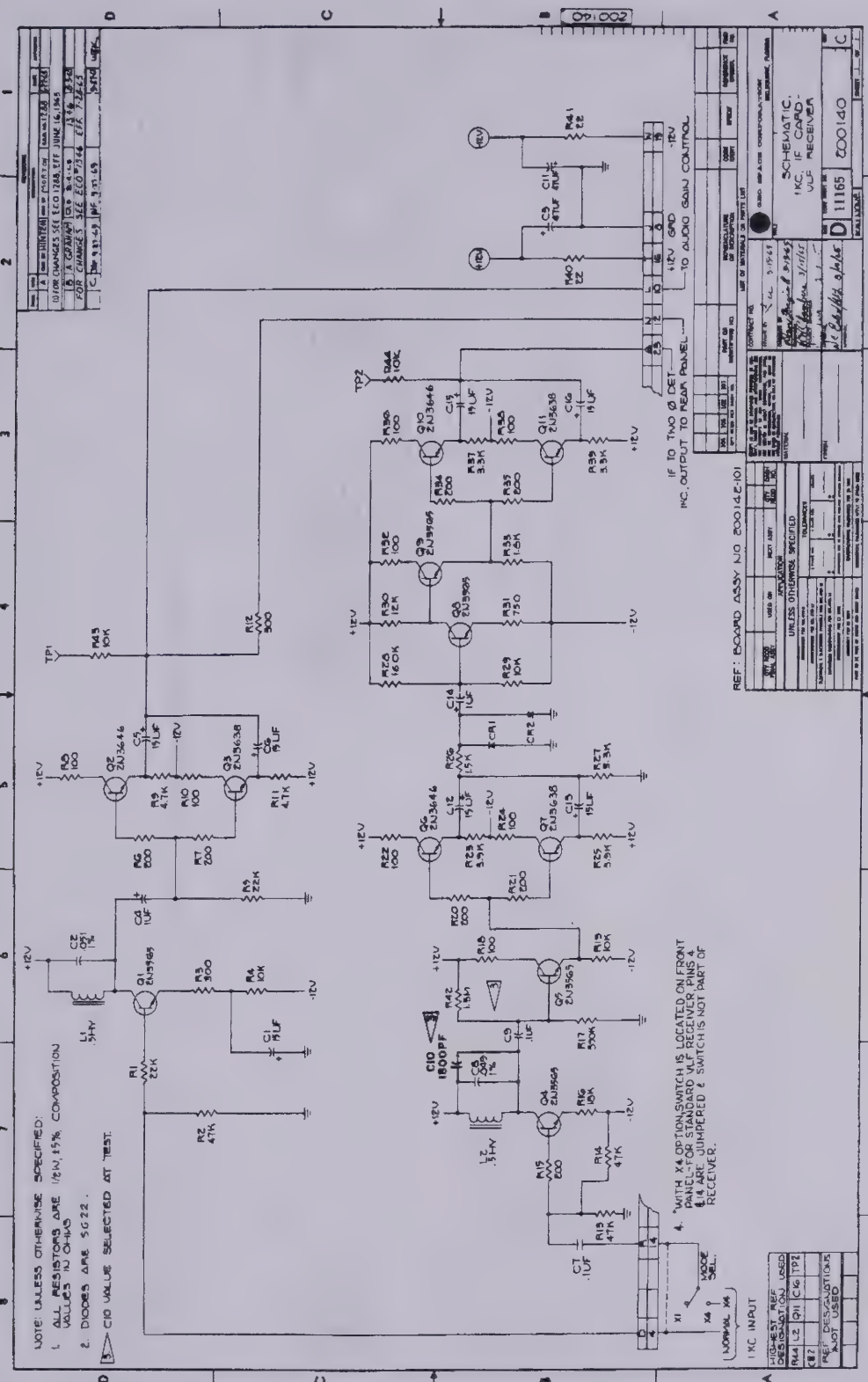

SCHEMATIC,
1KC, IF AMP.
VLF
RECEIVER
D 11165 200140
REF: BOARD ASSY NO 200142-101
IF TO TWO Ø DET
1KC. OUTPUT TO REAR PANEL
+12V GND
-12V
TO AUDIO GAIN CONTROL
1KC INPUT
NOTE: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/2W, 5% COMPOSITION VALUES IN OHMS
2. DIODES ARE 1S22.
3. C10 VALUE SELECTED AT TEST.
4. *WITH X4 OPTION SWITCH IS LOCATED ON FRONT PANEL FOR STANDARD VLF RECEIVER. PINS 4 & 14 ARE JUMPERED & SWITCH IS NOT PART OF RECEIVER.
MODE SEL.
NORMAL X4
X1
HIGHEST REF DESIGNATION USED
R44 L2 Q11 C16 TP2
REF DESIGNATIONS NOT USED
E1L5895-413-15/3-27

*Figure 3-22. Schematic, 1-kc IF amplifier assembly, A16*

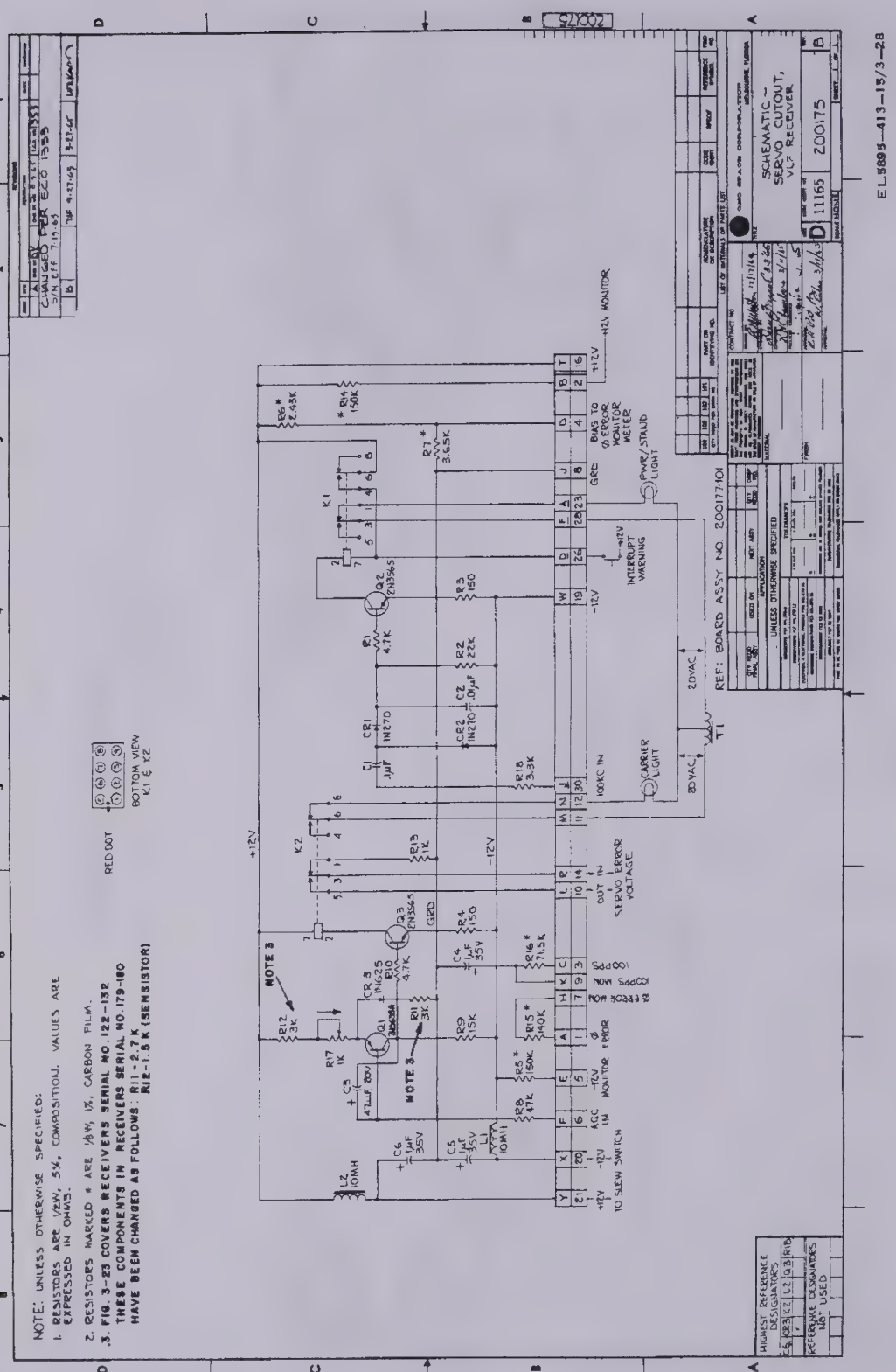

SCHEMATIC
SERVO CUTOUT,
VCF RECEIVER
D 11165 200175
EL5895-413-15/3-28
REF: BOARD ASSY NO. 200177-101
NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/2W, 5%, COMPOSITION. VALUES ARE EXPRESSED IN OHMS.
2. RESISTORS MARKED * ARE 1/8W, 1%, CARBON FILM.
3. FIG. 3-23 COVERS RECEIVERS SERIAL NO. 122-132. THESE COMPONENTS IN RECEIVERS SERIAL NO. 179-180 HAVE BEEN CHANGED AS FOLLOWS: R11 - 2.7 K R12 - 1.5 K (SENSISTOR)
BOTTOM VIEW K1 & K2
RED DOT
+12V
-12V
20VAC
100KC IN
SERVO ERROR VOLTAGE
+12V MONITOR
INTERRUPT WARNING
CARRIER LIGHT
PWR/STAND LIGHT
BIAS TO DETECTOR VOLTAGE METER
NOTE 3

*Figure 3-23. Schematic, servo cutout assembly, A17*

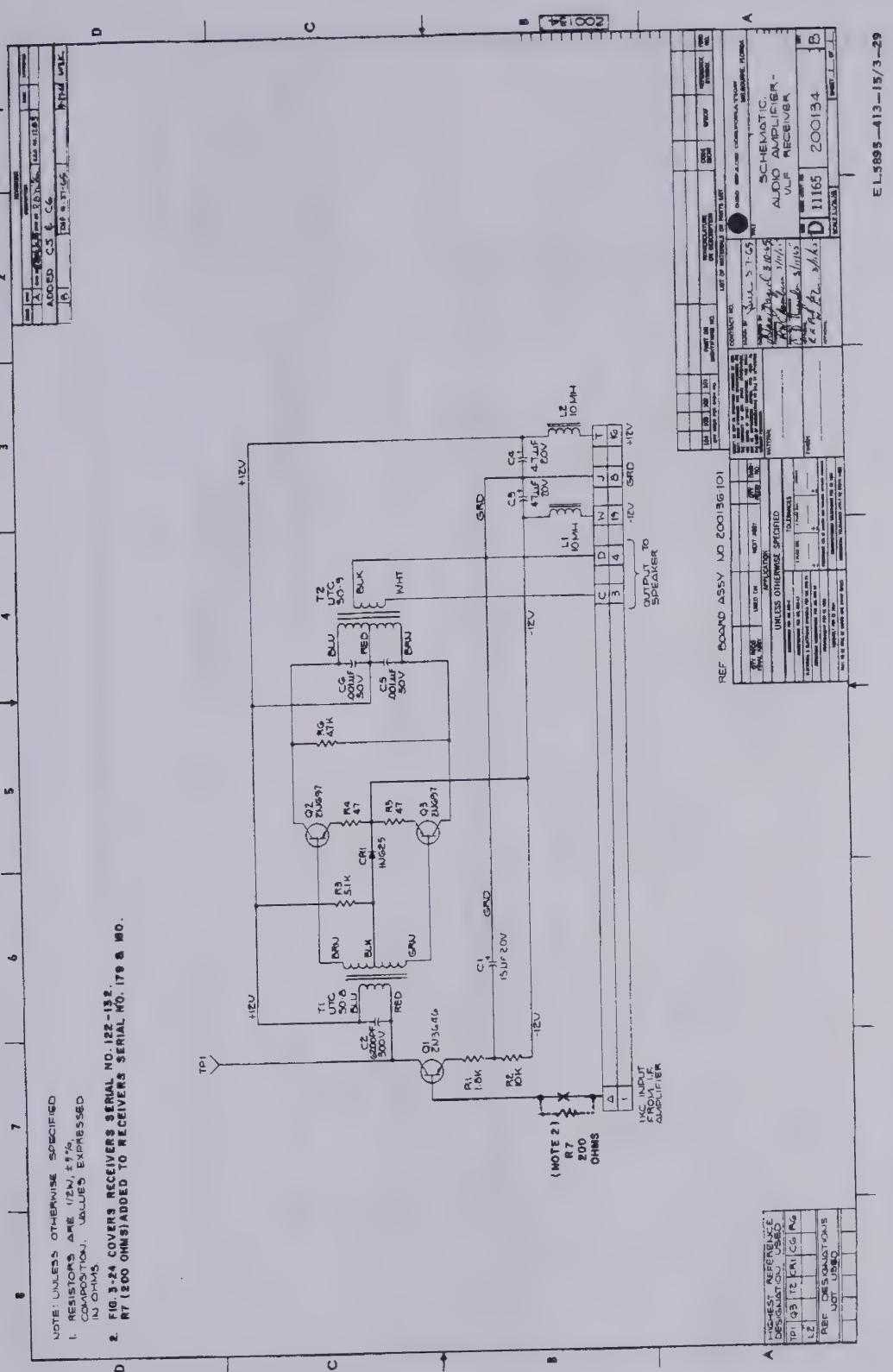



*Figure 3-24. Schematic, audio amplifier assembly, A19*

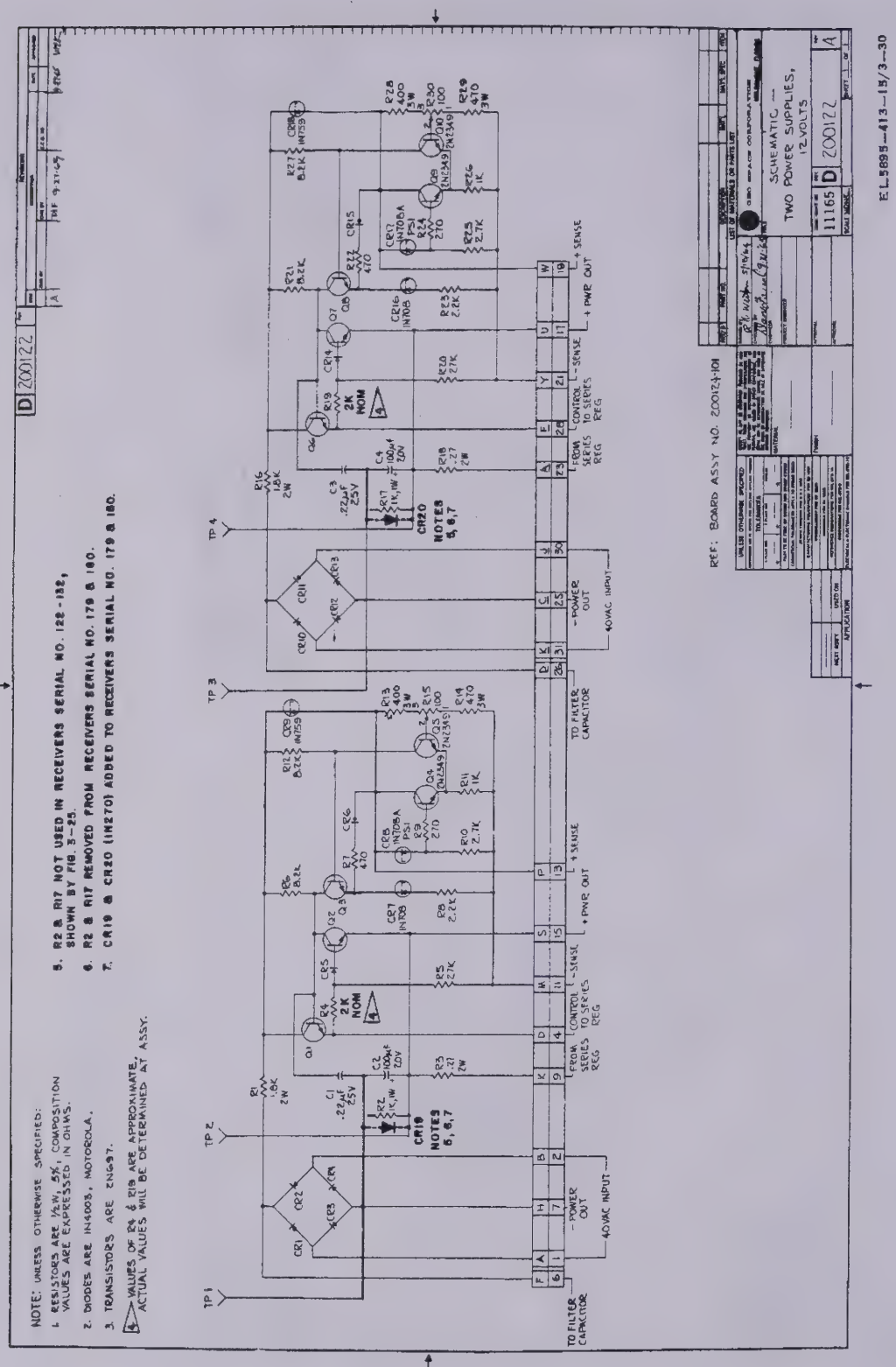

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE ½W, 5%, COMPOSITION VALUES ARE EXPRESSED IN OHMS.
2. DIODES ARE IN4003, MOTOROLA.
3. TRANSISTORS ARE 2N697.
4. VALUES OF R4 & R19 ARE APPROXIMATE, ACTUAL VALUES WILL BE DETERMINED AT ASSY.
5. R2 & R17 NOT USED IN RECEIVERS SERIAL NO. 122-132, SHOWN BY FIG. 3-25.
6. R2 & R17 REMOVED FROM RECEIVERS SERIAL NO. 179 & 180.
7. CR19 & CR20 (1N270) ADDED TO RECEIVERS SERIAL NO. 179 & 180.
D 200122
TP1
TP2
TP3
TP4
CR19 NOTES 5, 6, 7
CR20 NOTES 5, 6, 7
2K NOM
- POWER OUT
40VAC INPUT
TO FILTER CAPACITOR
FROM SERIES REG CONTROL TO SERIES REG
+ PWR OUT
+ SENSE
- SENSE
FROM SERIES REG CONTROL TO SERIES REG
+ POWER OUT
40VAC INPUT
TO FILTER CAPACITOR
REF: BOARD ASSY NO. 200124-101
SCHEMATIC — TWO POWER SUPPLIES, 12 VOLTS
11165 D 200122
EL5895-413-15/3-30

*Figure 3-25. Schematic, plus and minus 12-volt power supply assembly, A20*

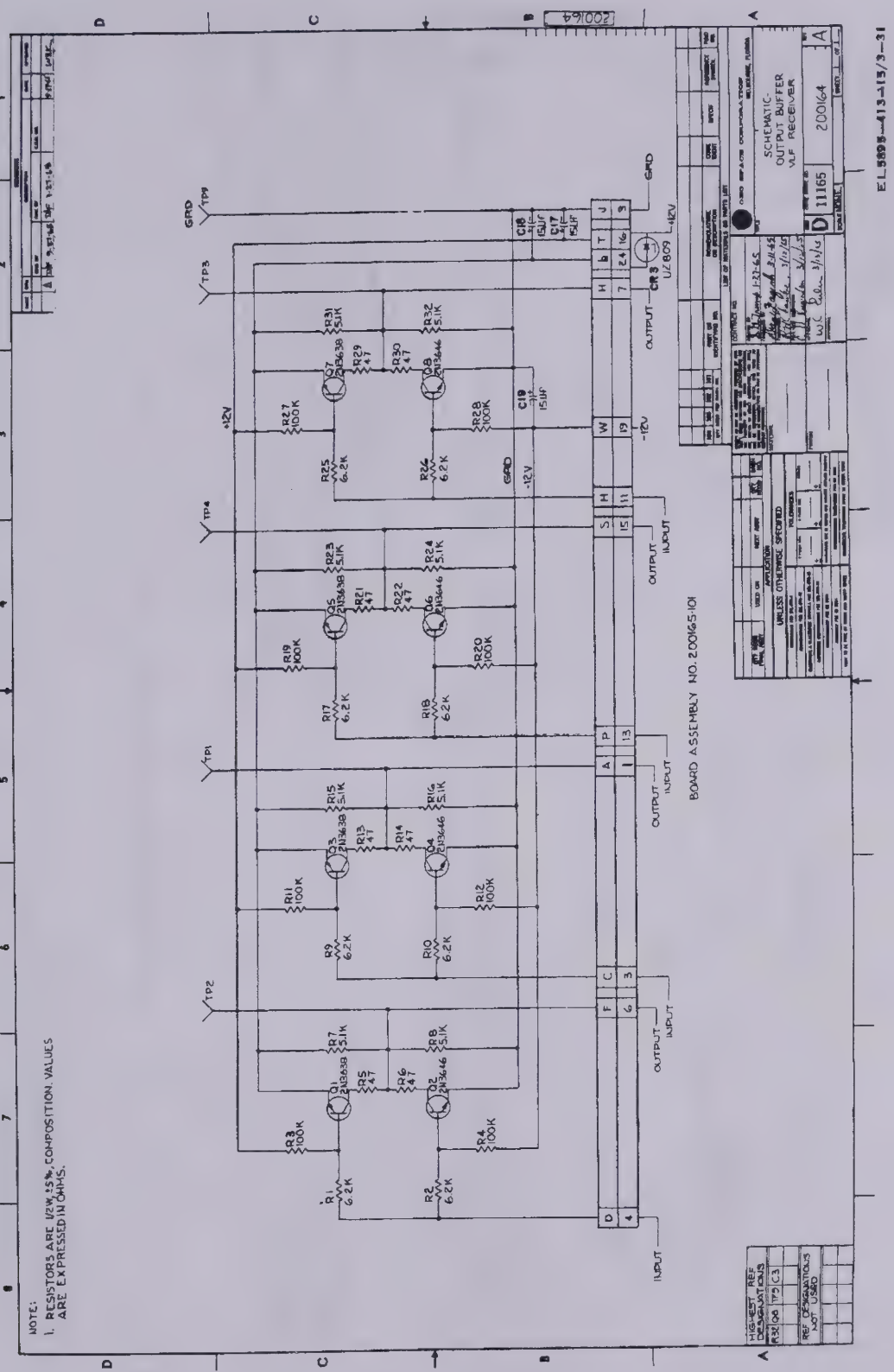



*Figure 3-26. Schematic, output buffer assembly, A25*

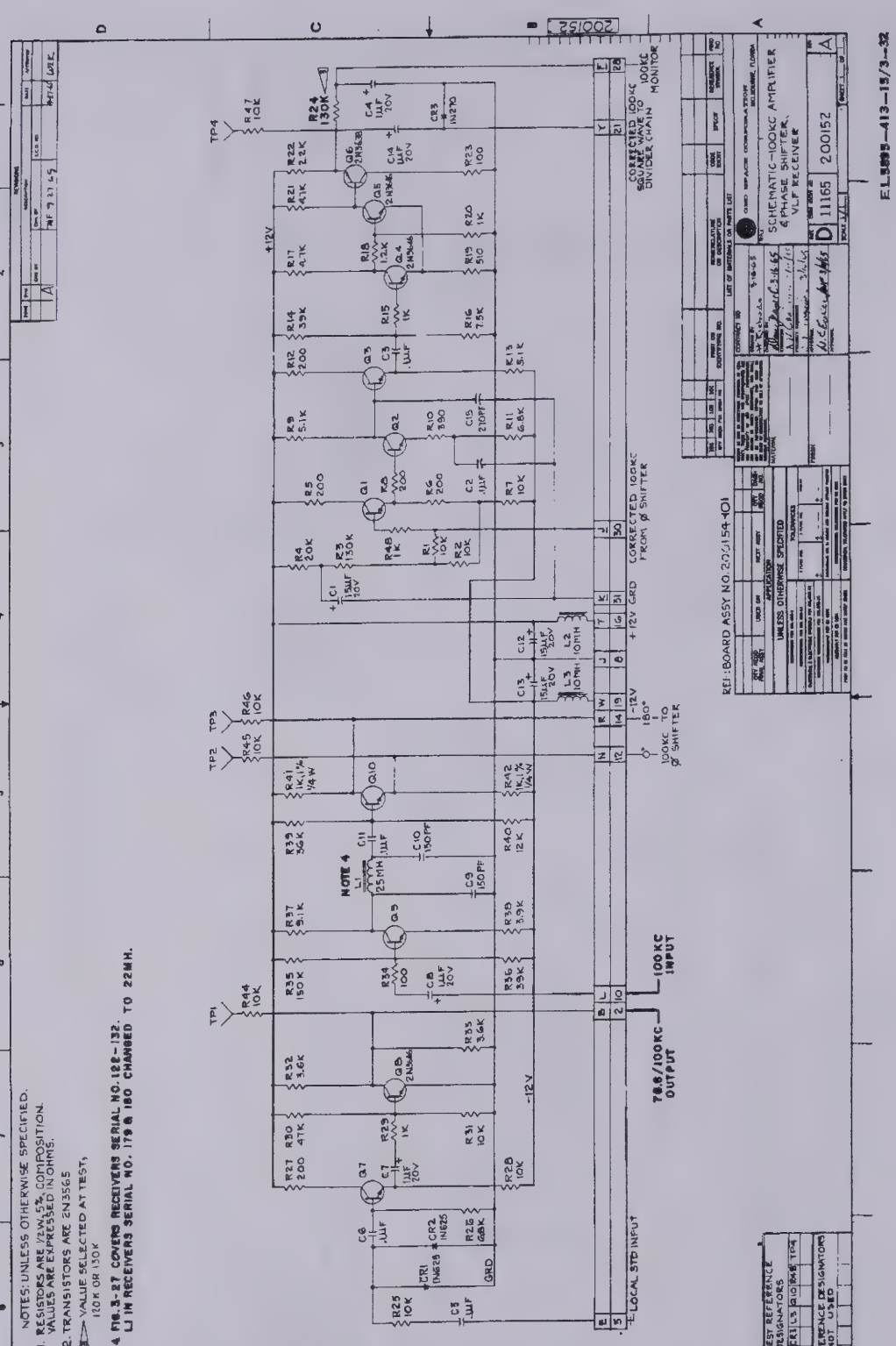
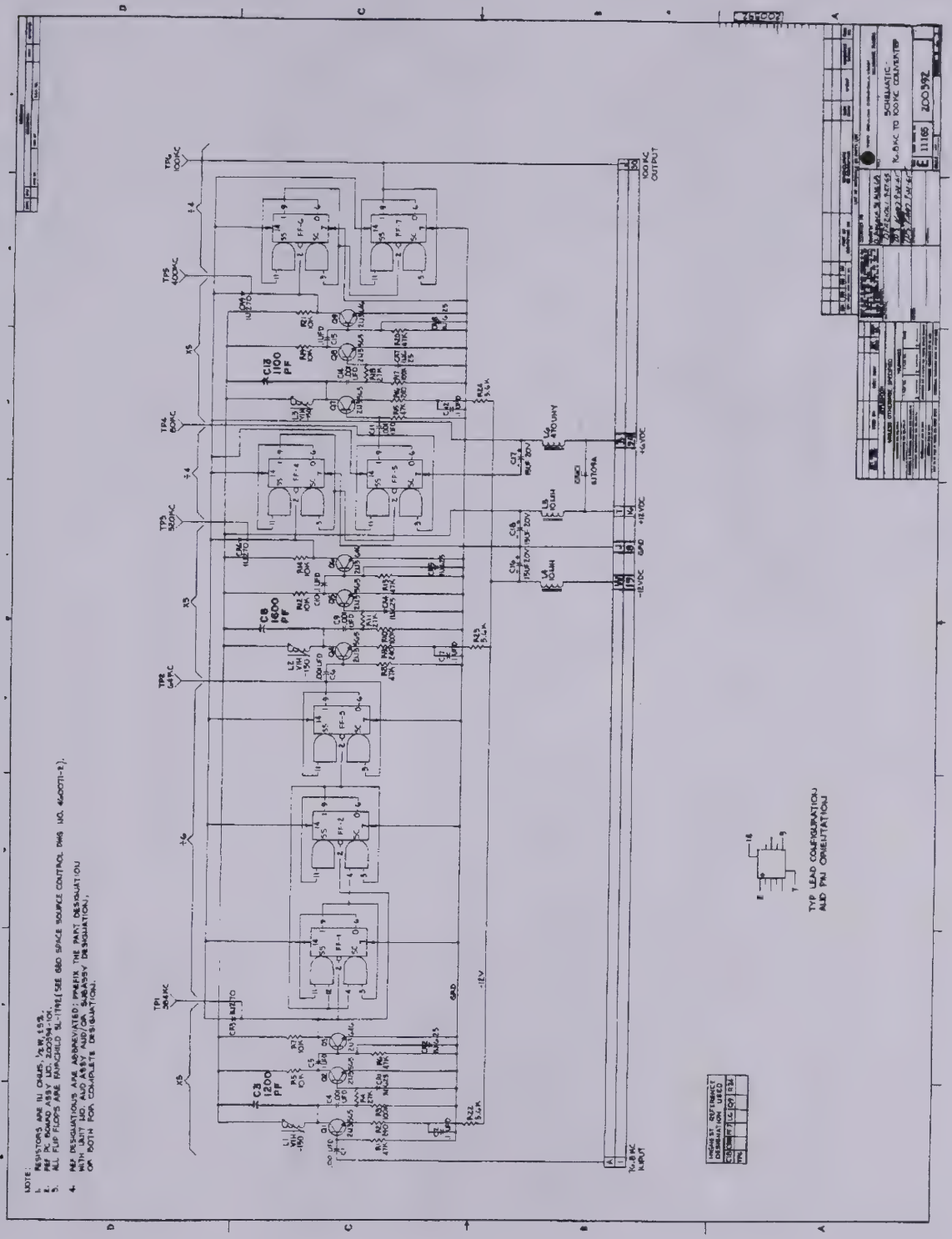

NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/2W, 5% COMPOSITION. VALUES ARE EXPRESSED IN OHMS.
2. TRANSISTORS ARE 2N3565
VALUE SELECTED AT TEST; 120 K OR 130 K
4 FIG. 3-27 COVERS RECEIVERS SERIAL NO. 182-132. L1 IN RECEIVERS SERIAL NO. 179 & 180 CHANGED TO 22MH.
REI: BOARD ASSY NO. 200154-101
SCHEMATIC-100KC AMPLIFIER & PHASE SHIFTER, VLF RECEIVER
D 11165 200152 A
CORRECTED 100KC SQUARE WAVE TO 100KC DIVIDER CHAIN MONITOR
CORRECTED 100KC FROM ϕ SHIFTER
+12V GRD
-12V
180° 100KC TO ϕ SHIFTER
100KC INPUT
70.6/100KC OUTPUT
LOCAL STD INPUT
HIGHEST REFERENCE DESIGNATIONS
REFERENCE DESIGNATIONS NOT USED
EL 5895-413-15/3-32

*Figure 3-27. Schematic, 100-kc amplifier and phase shifter assembly, A14*



EL5895-413-15/3-33

*Figure 3-28. Schematic, 76.8 to 100-kc converter assembly, A24*

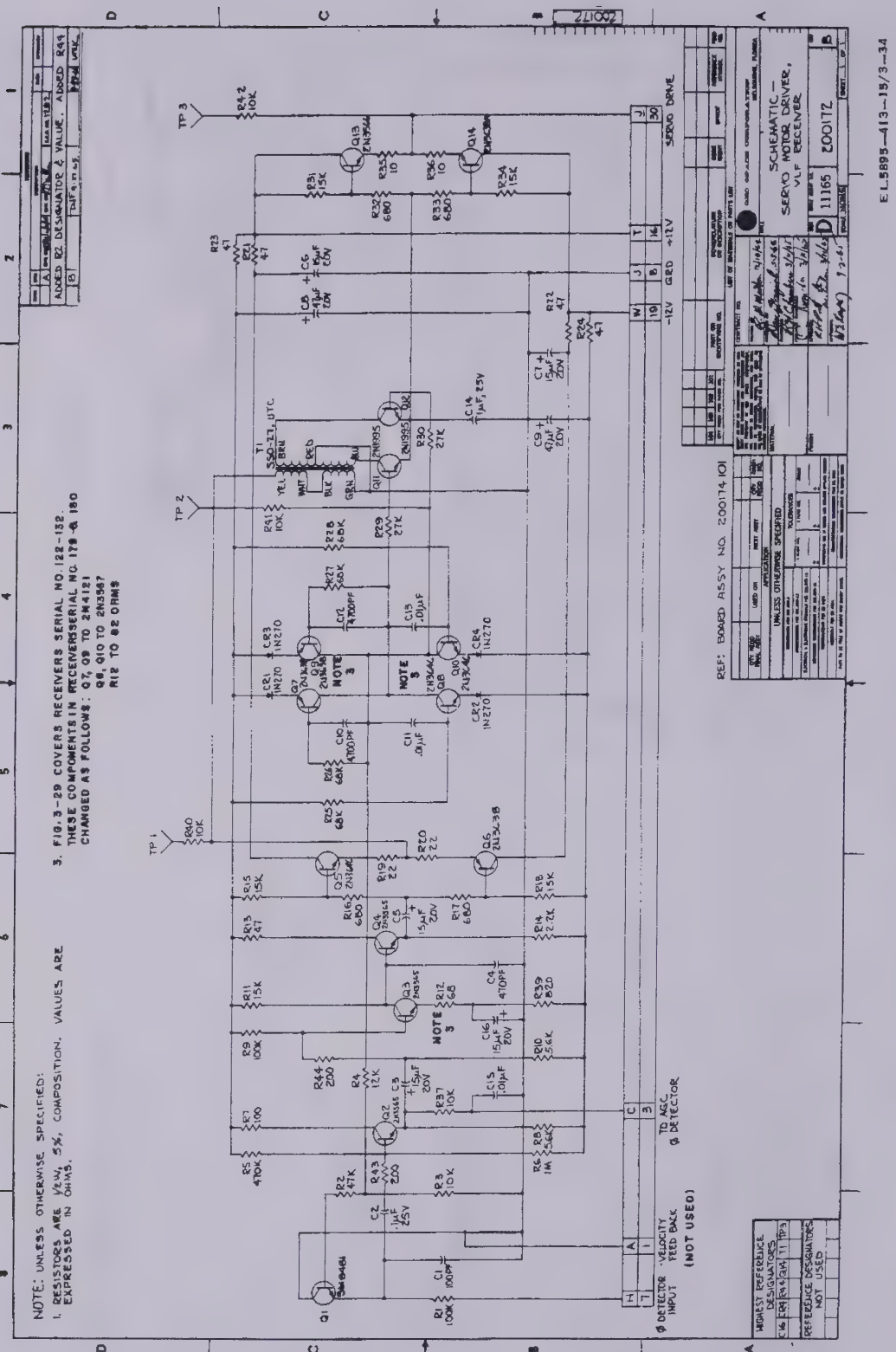

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE ½W, 5%, COMPOSITION. VALUES ARE EXPRESSED IN OHMS.
3. FIG. 3-29 COVERS RECEIVERS SERIAL NO. 122-132. THESE COMPONENTS IN RECEIVERS SERIAL NO. 178 & 180 CHANGED AS FOLLOWS: Q7, Q9 TO 2N4121 Q8, Q10 TO 2N3567 R12 TO 82 OHMS
REF: BOARD ASSY NO. 200174-101
SCHEMATIC - SERVO MOTOR DRIVER, VLF RECEIVER
11165
200172
SERVO DRIVE
Φ DETECTOR - VELOCITY FEED BACK INPUT (NOT USED)
TO AGC Φ DETECTOR
E.L. 5895-413-15/3-34

*Figure 3-29. Schematic, servo-motor driver assembly, A18*

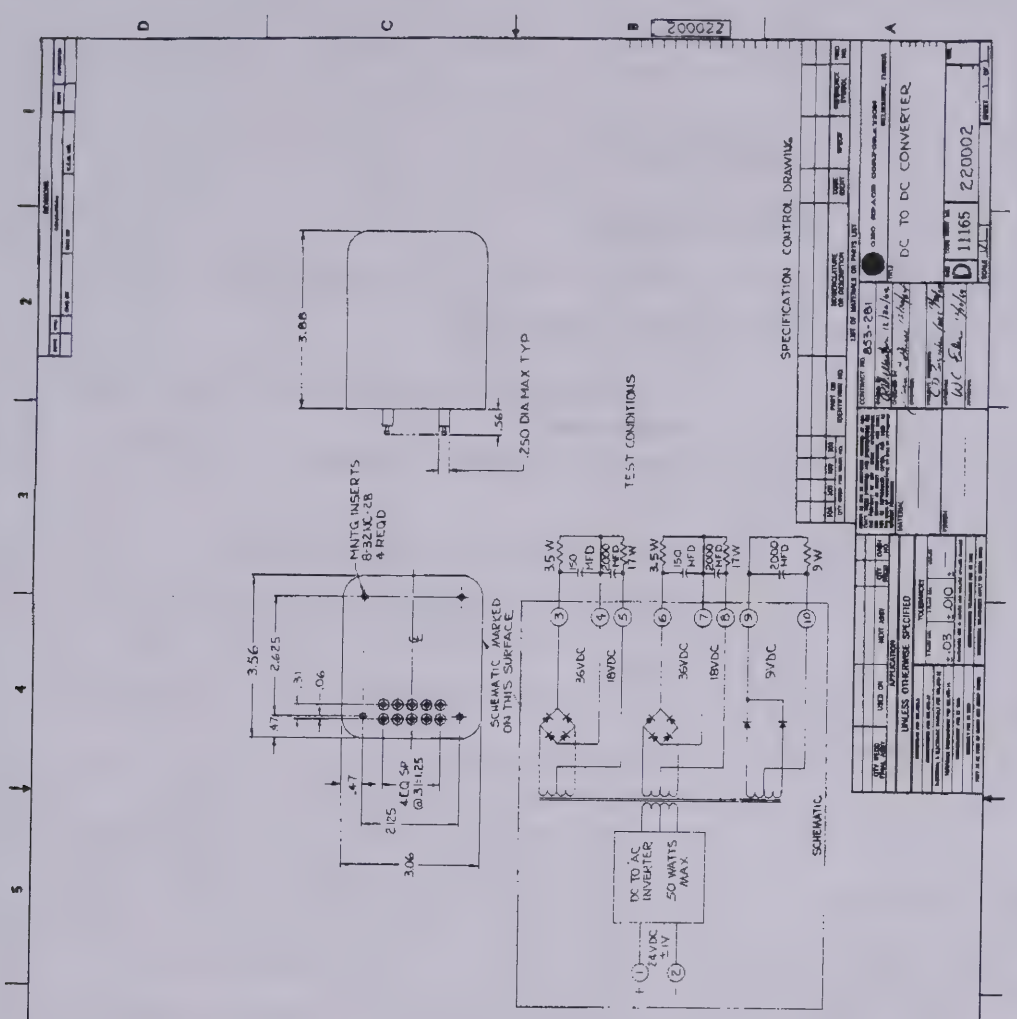

NOTES:
1. TRANSFORMER SHALL MEET THE SPECIFICATION REQUIREMENTS OF MIL-T-27 INCLUDING THE FOLLOWING:
A. MARKING SHALL BE IN ACCORDANCE WITH MIL-STD-130.
B. FINISH SHALL MEET TYPE II EXPOSURE OF MIL-F-14072.
C. COLOR SHALL CORRESPOND TO COLOR SPECIFIED IN MIL-E-15090.
2. NOMINAL VOLTAGE ACCURACY ±5%.
3. DIMENSIONS SHOWN ARE MAXIMUM. A SMALLER CASE IS DESIRED IF COMPATIBLE WITH COST, ENVIRONMENT, AND GOOD ENGINEERING PRACTICES.
DESIGN INFORMATION:
1. EACH INDIVIDUAL WINDING SHALL BE DESIGNED TO HANDLE 1 AMP OF CURRENT CONTINUOUS DUTY. THE COMBINED OUTPUT LOAD OF ALL WINDINGS SHALL NEVER EXCEED 80 WATTS TOTAL.
2. REVERSE POLARITY PROTECTION SHALL BE PROVIDED AT THE DC INPUT. INPUT SHALL BE ISOLATED FROM THE CASE & OUTPUTS. (100V MIN ISOLATION)
3. OUTPUT RIPPLE SHALL BE HELD TO LESS THAN 0.15 VPP AT THE 36V OUTPUTS, LESS THAN 0.15 VPP AT THE 18V OUTPUTS, AND LESS THAN 0.25 VPP AT THE 9V OUTPUT. THE RIPPLE MEASUREMENT SHALL BE MADE USING THE EXTERNAL CAPACITOR ARRANGEMENT SHOWN AS A PART OF THE SCHEMATIC.
4. INPUT TO OUTPUT EFFICIENCY AT 50 WATT LOAD SHALL NOT BE LESS THAN 80% NO-LOAD INPUT CURRENT SHALL NOT EXCEED 350 MA.
5. SHORT CIRCUIT PROTECTION IS DESIRED. IF THIS IS ECONOMICALLY OR TECHNICALLY INADVISABLE THE CONVERTER SHALL BE ABLE TO WITHSTAND AT LEAST 30 SECONDS AT 150% RATED LOAD AND/OR 10 SECONDS WITH ONE OF THE OUTPUTS SHORT CIRCUITED.
6. THE CONVERTER SHALL OPERATE OVER A TEMPERATURE RANGE OF -30° TO +75°C MOUNTED TO A CHASSIS HAVING A 16 INCHES IN SIDE AND IN FREE AIR. CONVERTER SHALL NOT FAIL TO START AT -30°C AFTER SATURATING AT THIS TEMPERATURE FOR 24 HOURS.
7. CONVERTER FREQUENCY SHALL NOT EXCEED 2KC.
8. CONVERTER NOT SUPPLIED WITH RECEIVERS SERIAL NO. 178 & 180.
MNTG INSERTS 8-32 UNC-2B 4 REQD
.250 DIA MAX TYP
SCHEMATIC MARKED ON THIS SURFACE
TEST CONDITIONS
DC TO AC INVERTER
50 WATTS MAX
24VDC ±1V
36VDC
18VDC
9VDC
SCHEMATIC
SPECIFICATION CONTROL DRAWING
DC TO DC CONVERTER
D 11165
220002
EL 5895-413-15/3-35

*Figure 3-30. Schematic, dc-to-dc converter*

# CHAPTER 4

# MAINTENANCE

## Section I. PREVENTIVE MAINTENANCE

### 4-1. General

This chapter provides instructions for the preventive maintenance, corrective maintenance, removal and replacement, and alignment and calibration of the vlf-12B. The printed-circuit card approach utilized in the construction of the vlf-12B provides a rapid yet simple method of maintenance. If a failure should occur, it may quickly be isolated to a malfunctioning card assembly and this card replaced. The defective card assembly may then be subjected to trouble analysis without having the equipment inoperative for any length of time.

### 4-2. Scope of Preventive Maintenance

*a.* Preventive maintenance consists essentially of cleaning and general inspection of the unit to maintain the best environment for equipment operation. The frequency of this periodic maintenance is given where applicable or useful. Procedural instructions are also given as appropriate for the period maintenance.

*b.* When used in a normal or controlled environment, the vlf-12B can be expected to operate properly for long periods with little or no maintenance required. However, it is expected that the operating personnel will be concerned with attending to the physical condition of the equipment, with checking for evidence of damage and wear, and with making certain component replacements, repairs, and adjustments. These functions include:

(1) Visual and operational inspection of the equipment, cabling, and connections

(2) Operational check of functions and controls

(3) Replacement of lamps, fuses, and chart paper

(4) Repair of coaxial and multiconductor cabling

### 4-3. Tools and Materials Required

The following tools and materials are required for proper performance of preventive maintenance:

*a.* A set of common hand tools consisting of:

(1) Screwdriver, 6 by 1/4 inch
(2) Diagonal cutter, 4 or 6 inches
(3) Needle-nose pliers, 4 or 6 inches
(4) Soldering iron, 30-watt, pencil-type
(5) Wrench, open-end, adjustable
(6) Brush, bristle, 2-inch
(7) Wrench set, hexagonal-head
(8) Card extraction tool

*b.* Several patches of clean cloth, approximately 4 by 4 inches.

*c.* Cleaning compound for cleaning electrical contacts.

### 4-4. Preventive Maintenance Procedures

*a. General.* Preventive maintenance entails the inspection and cleaning of the vlf-12B. Most of the unit components require only minor attention from time to time, as they are designed to be relatively independent and accordingly fail-safe. Inspections, for the most part, are visual, and will detect and substandard conditions of those items that require special attention on a periodic schedule. The major areas of concern to a periodic maintenance plan are given in paragraphs 4-4*b* through 4-4*e*. The procedures are given in paragraphs 4-4*f* through 4-4*h*.

*b. Lubrication and Oiling.* The mechanical moving parts in the vlf-12B that require lubrication have been previously lubricated with a permanent-type lubricant of high quality.

*c. Cleaning.* Cleaning can be a major factor affecting the life of the equipment, and in general will save a lot of equipment downtime and unnecessary damage. A few recommendations are listed below.

(1) Each time an assembly or unit is repaired or handled, clean up the associated litter and subject item.

(2) Loosely coil test leads and cables; then store them where they are neat and convenient for next usage.

(3) Clean or wipe the panels, instruments, switches, control knobs, glass etc.

(4) Do not handle dial faces, panels, or controls without reason, because grease and foreign matter on the hands is deposited in this manner and contributes to the overall unsightly condition of the equipment.

(5) Dust around all equipment areas daily.

(6) Vacuum dust from all assemblies by using a high-powered vacuum cleaner or blower to remove accumulations of dirt and dust from all assemblies, printed-circuit cards, modules, and components. Give particular attention to the bottom of each cabinet, and make sure that all dirt and foreign matter are removed.

*d. Periodic Inspections.* Periodic inspections of the vlf-12B are essentially divided into two categories. These are visual examination and operational checkout of the equipment. The visual examination should include a check of all of the cables and wiring in the equipment on a monthly basis for signs of fraying or damage. Without the equipment operating, manipulate all knobs, switches, and controls while observing them for unnecessary play or looseness in action. Check electrical connections for secure mounting; tighten lugs and terminals where needed. Check all painted surfaces for evidence of scratching, grazing, or chipping. Unusual discoloration should be reported or logged in a suitable manner. All panel lettering is embossed by a special photographic process, and then sprayed with a protective coating. At the appropriate parts locations on the chassis, printed-circuit cards, etc, components are identified with suitable reference designations in black ink that has been stamped and then covered with a protective clear lacquer. Therefore, an inspection which reveals unsatisfactory appearance with regard to the panel finishes should be corrected at the first opportunity. Usually, retouching various painted surfaces can be accomplished during the time of a routine equipment shutdown. Deep chips and scratches may require more than one retouching application to obtain a desired finished appearance. Another phase of visual periodic inspection includes an examination of all broken hardware and accessories that may not affect the electronic operation of the equipment. Their replacement, however, should be facilitated as soon as appropriate without constituting a specific equipment shutdown. Each item of hardware selected for use in the equipment has some functional purpose that has been provided for the ease of maintenance or operation by the associated personnel, and therefore should be kept in as ready a state as practicable.

*e. Schedules.* Periodic inspection of the vlf-12B should be scheduled as a preventive maintenance measure on a monthly basis. However, the interval may be changed, depending upon the nature of the operating environment. If the equipment is subjected to a dirty or corrosive atmosphere or if vibration transmitted to the equipment is significant, the visual and operational inspection and cleaning should be scheduled on a weekly basis. The various lamps and fuses are to be replaced on an "as required" basis. However, if a fuse should burn out, further inspection of the equipment should be made to check for possible damage to the equipment that caused the burnout. The recorder chart paper is also replaced on an "as required" basis.

*f. Visual and Operational Inspection and Cleaning.* With power to the equipment removed, check thoroughly for dirt, dust, and corrosion. Use a soft-bristle brush to remove accumulations of dust and dirt on interior and exterior surfaces and on the readily accessible printed-circuit boards and wafer switches. Check all controls for loose knobs and for

binding or looseness against the panel mountings. After the pre-operational checks are performed and while power is still applied to the equipment, manipulate all cables and connectors; observe the front panel indicators for evidence of erratic or interrupted operation that may be due to a faulty connection. When necessary, repair the coaxial or multiconductor cables according to the procedures shown in figures 4-1 and 4-2, respectively.

*g. Replacement of Lamps and Fuses*

(1) Replace the INTERRUPT WARNING indicator lamps as follows:

(*a*) Grasp the switch cover plate firmly with the fingers and pull the light assembly straight out from the front panel.

*Note.* Be careful not to loose name plates or lamp covers.

(*b*) Remove the burned-out lamp from the rear of the lamp assembly by grasping it with the fingers and pulling straight out.

(*c*) Press the new lamp into the socket of the lamp assembly.

(*d*) Replace the entire assembly into the socket by pushing it straight in, as far as it will go.

(2) Replace a burned-out fuse as follows:

(*a*) Grasp the fuseholder with the fingers and turn it counterclockwise 1/4 turn; then withdraw the fuseholder with the blown fuse.

(*b*) Remove the defective fuse from the holder. After determining and repairing the trouble causing the fuse to blow, replace the fuse with a new fuse of identical value.

(*c*) Replace the fuseholder by pushing it against the spring tension of the socket, and then turning the holder clockwise 1/4 turn. The entire holder should remain locked into the socket.

*h. Chart Paper Loading.* Replace the chart paper by utilizing the following procedure, illustrated in figure 4-3:

***Caution:* When loading chart paper, remove equipment power.**

(1) At the lower-right corner of the panel, loosen the knurled thumbscrew and open the panel until the catch engages the panel in the raised position.

(2) Push up the two retaining clips; then remove both the empty supply spool and the take-up spool from their slots.

(3) Place a new roll of chart paper on the supply roll in such a manner that the perforations in the paper are adjacent to the knurled shoulder of the roller.

(4) Remove the masking tape from the roll of chart paper; the masking tape may be retained for later use.

(5) With the back (dark) side of the paper facing you, roll out approximately 8 inches of paper from the supply roll.

(6) Use the masking tape removed in step (4) to attach the end of the paper to the cardboard tube on the take-up spool. Be sure to keep the edges of the paper parallel with the edges of the cardboard tube.

(7) With the graph side of the paper visible, roll the paper onto the takeup spool.

(8) Using both hands, as shown in figure 4-3, slide the paper into the recorder until the holes in the paper engage the sprockets on the drive drum. Without tearing the paper perforations, hold the paper taut against the drive drum. Be sure to keep the paper above the pointer guard.

*Note.* Exercise care during the loading steps to prevent snagging the stylus with the chart paper.

(9) Depress the brake and insert the full supply roll into the two upper slots on the metal frame.

(10) Take up any slack by rolling the excess paper around the take-up spool; then insert the partially loaded take-up spool into the two lower slots on the metal frame.

(11) With both the supply roll and the take-up spool in their respective slots, push down the two retaining clips to their locked positions.

(12) Release the locking catch holding the panel in the raised position, and then lower the panel to the closed position and tighten the knurled thumbscrew.

## Section II. CORRECTIVE MAINTENANCE

### 4-5. General

*a.* Corrective maintenance (trouble analysis) is presented to isolate malfunctions to a particular circuit in the vlf-12B, and is intended to be performed by utilizing the various controls on the front panel and the test points of the printed-circuit cards. The vlf-12B, as with most sophisticated digital-logic electronic equipment, contains both solid-state and standard components. The isolation and remedy of all malfunctions are fairly straightforward, utilizing standard troubleshooting techniques. The major trouble analysis aids employed in these techniques are the block and schematic diagrams, the principles of operation contained in chapter 3, and the external signal generators and oscilloscopes. It is assumed that maintenance personnel will utilize the individual module schematics referenced in chapter 3 as an aid in trouble analysis.

*b.* All card assemblies, except the RF and IF, are provided with easily accessible test points after each circuit element. Rapid troubleshooting of the individual assemblies is thus facilitated by using the test points in conjunction with the schematic diagrams. A malfunction can generally be localized to a particular circuit by using the test points provided. When a malfunctioning card assembly is replaced by a spare, the test that isolated the assembly should be repeated to ascertain that the replacement is operating properly.

*c.* Examples of typical trouble analysis are given in the following paragraphs and table 4-1. These paragraphs present the method of suggested trouble analysis that can be used to detect, localize, and isolate the equipment malfunctions. They also provide suggested remedies for the correction of the typical malfunctions; they are not intended to be considered as the only way to analyze malfunctions, but are intended to serve as procedural guides to the overall troubleshooting methods. In addition to the suggested typical trouble analysis paragraphs, it is necessary to use the block and schematic diagrams and other such material as required to follow a malfunction to its point of origin.

*d.* Trouble analysis of equipment malfunctions is to be performed from the test points and front panel controls as a first step. From this point, block and schematic diagrams are utilized to localize and isolate the malfunction and effect a satisfactory remedy. When the remedy appears satisfactory, test the operation of the repaired part of the equipment by performing the applicable portion of its operational procedure. Localization of malfunctions and remedies are dependent upon the skill of maintenance personnel. Logical go and no-go approaches to trouble isolation are recommended as the most efficient trouble-analysis procedures. Troubleshooting the equipment generally requires standard signal tracing and the use of some circuit-substitution techniques. The functional block diagrams and schematic diagrams aid in narrowing the location of a malfunction to a component on a particular card assembly, and should be consulted at all times. Repair can usually be effected by replacement of the faulty card assembly or component from a reserve supply. The following are general recommendations for troubleshooting and repair:

(1) When possible, troubleshoot the equipment with power OFF. When required to troubleshoot with energized equipment, exercise care to avoid accidental grounding, short circuit, or arc-over that may further damage the equipment, and also complicate trouble analysis and repair.

(2) During all troubleshooting and repair procedures, use soldering irons, other hand tools, test equipment, and test probes carefully to avoid short circuits, grounds, or mechanical damage to the wiring of components. After repairs, restore lead installation to its original condition.

(3) When pulling out, or pushing in, slide-mounted card assemblies, position carefully to avoid damage. Do not attempt to remove card assemblies without the use of an extraction tool, as damage could result to the card assembly or its associated pin sockets.

(4) With due regard to the general mechanical ruggedness of diodes and transis-

tors, these devices can be destroyed or permanenty damaged by the effects of heat and electrical overload that could accidently be applied during routine maintenance and checkout. Transistor and diode circuits are frequently sophisticated in design and operation, and trouble analysis and repair for these circuits can be complicated by such hidden damage.

(5) When soldering transistor or diode leads to printed-circuit terminals, use a grounded heat sink to prevent damage that could be caused by heat or the leakage of electrical current. A grounded heat sink might consist of a short length of heavy, insulated, flexible wire with an alligator clip soldered to each end. Before soldering the subject diode or transistor leads, connect one of the alligator clips to the transisor or diode lead between the body of the device and the point to be soldered, when possible. Ground the other alligator clip to the chassis.

(6) When soldering near a diode or transistor, place a piece of thermal insulating material between the soldering iron and the device, to prevent heat damage.

(7) When a card assembly is suspected of being malfunctioning, it should be replaced by one of the same type that is known to be good. In the event that suitable card spares of the type required are not available, it is advisable to have an equipment log placed on each rack or cabinet to record when one is removed from another equipment for substitution. This "notice" method if card assembly removal should describe the type of card, give its location, and bear the date and signature of the responsible person. In this way, unnecessary trouble analysis and malfunction isolation are avoided.

(8) Paragraph 4–6*a* provides a step-by-step procedure that may be used as an operational check of the vlf-12B, or utilized as a troubleshooting test to localize malfunctions to a card assembly. Before performing any of the tests given in the following paragraphs, the usual preliminary checks should be made. That is, make sure that all power is correctly applied, that all equipment is energized, and that all controls are properly positioned on all units. Paragraphs 4–6*b* through 4–6*e* are further troubleshooting procedures that can be utilized for isolating malfunctions to an individual component. Alignment and calibration procedures for the vlf-12B are given in paragraph 4–8. The removal and installation instructions are provided in paragraph 4–7.

## 4–6. Trouble Analysis Procedures

*a. General.* A logical step-by-step procedure should be followed in isolating a malfunction in any electronic equipment. The first step in intelligent troubleshooting is to become familiar with the principles of operation of the equipment. Chapter 3 of this volume contains the theory of operation for the vlf-12B. Once the theory is thoroughly understood, troubleshooting can proceed. The following subparagraphs detail the methods to be used with the vlf-12B.

***Warning:*** **When troubleshooting the vlf-12B, use caution at points of high voltage. Although the highest voltage utilized is approximately 120 vac, caution should be exercised in working with the equipment. Many deaths have resulted from ONLY 120-vac lines. If no voltage or waveform measurements are to be made, disconnect the main power.**

(1) *Operational check.* Many troubles can be isolated by using the operational check. Refer to chapter 2 of this volume for the operating instructions and the preoperational check procedure. The vlf-12B contains six key test points that con be monitored by a front panel meter and selected by the METER FUNCTION switch. Additional localization can be obtained by observing the CARRIER and PWR/STD indicators and by monitoring the audio output of the speaker on the front panel. Table 4–1 provides operational checks; it lists the check to be performed, the normal indication that should be obtained, and a possible malfunction that could prevent the normal indication.

(2) *Localization of fault to a specific assembly.* The vlf-12B is basically constructed of plug-in circuit modules on printed-circuit cards. This method of construction is utilized for ease in maintenance. Figure 3–9 illustrates a top view of the unit, with the covers removed,

to show the location of all printed-circuit cards.

(3) *Waveform check.* If the malfunction cannot be isolated to a specific module through the operational check or the functional check, utilize an oscilloscope to observe the waveforms of the various operating card assemblies. Paragraph 4–6*b* provides the procedure to use in waveform troubleshooting.

(4) *Signal substitution check.* The use of signal substitution checks is often very useful in localizing malfunctions in certain areas. This is especially true in the RF, IF, and audio sections. The method consists generally of injecting an audio or RF signal of known frequency and amplitude, from a signal generator or equivalent source, into the various input points, and then observing the output results. The procedure for this method is explained in paragraph 4–6c.

*Table 4–1. Operational Checks*

| Step | Functional check or symptom | Normal indication | Possible fault |
|---|---|---|---|
| 1 | Turn receiver power on. | POWER ON indicator should light. | Burned-out indicator lamp; ac power not connected; blown fuses usually indicate other internal problems. |
| 2 | Turn CHANNEL SELECTOR to a vlf station. | Station is heard on speaker, and receiver should begin tracking. As indicated on MICROSECONDS counter, CARRIER indicator lamp should be off. | Antenna disconnected; station not transmitting; attenuation set too high; defective RF or IF module. |
| 3 | METER FUNCTION selector on −12V. | Meter on red mark. | Power supply module (A20) not functioning. |
| 4 | METER FUNCTION selector on +12V. | Meter on red mark. | Power supply module (A20) not functioning. |
| 5 | METER FUNCTION selector on CARRIER. | Meter in green area; CARRIER lamp off. | IF and agc module (A16) not functioning when lamp is off and meter is not in green area. |
| 6 | METER FUNCTION selector on PHASE. | Meter in green area; receiver tracking. | Servo system not functioning. Check modules A14, A15, and A18. |
| 7 | METER FUNCTION selector on 100KC. | Meter in green area. | Check module A14. |
| 8 | METER FUNCTION selector on 100PPS. | Meter in green area. | Divider chain not working. Check output divider chain modules A21, A22, and A23. |
| 9 | Check for local standard input. | PWR STD indicator is off. | Indicator lamp burned out; local standard not functioning or disconnected. Module A14 or A24 not functioning. |
| 10 | Receiver tracking properly but no audio tone. | 1-kc audio from speaker. | Module A16 or A19 not functioning. |
| 11 | Clicking sound from speaker. | Normal 1-kc signal from vlf station. | Synthesizer not counting or locking properly. Check A7, A8, A9, A12, and A13. |
| 12 | Check SERVO selector on +SLEW. | MICROSECONDS counter advances. | Defective servo motor. |
| 13 | Check SERVO selector on −SLEW. | MICROSECONDS counter retards. | Defective servo motor. |
| 14 | Check SERVO selector on CUTOUT ON. | MICROSECONDS counter should return approximately to original position. | Servo motor, module A15, A18. |

(5) *Gain measurement check.* Some malfunctions that are difficult to isolate can often be found by making a gain measurement check. This method consists of measuring the gain (in decibels) of those stages where large variations in gain could produce improper operation. The procedures are explained in paragraph 4–6*c*.

(6) *Card assembly substitutions.* Once a malfunction is isolated to a card assembly, the faulty card can be replaced by one that is known to be good. Determination of the component(s) that is malfunctioning on the faulty card assembly can be made by utilizing the procedures given in paragraph 4–6*c*. For expediency in the field, where facilities are not available to allow repair of the individual card assemblies, it is recommended that the malfunctioning card assembly be replaced by a new card assembly.

*b. Waveform Trouble Analysis*

(1) In order to obtain the waveforms for trouble analysis, it is necessary to remove the top covers of the card assembly containers, thus exposing the test points. To assure proper waveforms, adjust the oscilloscope (Tektronix model 561A or equivalent) controls to obtain the settings given for each waveform shown in table 4–2. Small deviations due to component tolerances are to be expected. However, any major deviation in a waveform, or the lack of a waveform, indicates a malfunction in that card assembly, requiring further troubleshooting.

(2) Since the magnitude of their waveforms is too small to have any meaning, the RF and IF modules do not have test points available. To determine whether these modules are malfunctioning, monitor the front panel speaker for an audible output. A lack of audio output from the speaker indicates that the RF and IF stages are not functioning properly. The CARRIER indicator on the front panel is also energized, if the malfunction is due to the absence of the carrier. Troubleshooting of these stages is performed by signal substitution (para 4–6*c*).

(3) The frequency of the waveforms at the local oscillator varies by 100-cps increments, depending upon the position of the front panel thumbwheel CHANNEL SELECTOR switches. When the switches are operated to the 10.0-kc position, the local oscillator frequency is 22.25 kc, and when operated to the 30.0-kc position, the local oscillator frequency is 42.25 kc. When the 60-kc option is used, the local oscillator frequency is below the incoming 60-kc signal (60.00 kc – 12.25 kc = 47.74 kc). This corresponds to operating the thumbwheel CHANNEL SELECTOR switches to 35.5 kc; however, it is not necessary since the 60-kc position of the RANGE – KC control bypasses the thumbwheel switches and selects the proper divisor from the synthesizer to produce a local oscillator frequency of 47.75 kc. Since the voltage-controlled oscillator is operated at twice the local oscillator frequency, its output is 95.5 kc when the 60.0-kc channel is selected.

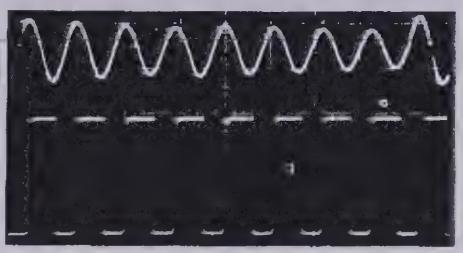
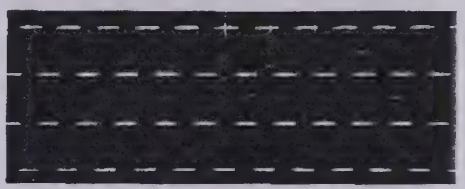
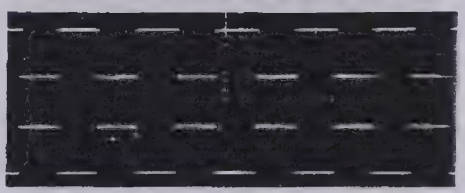
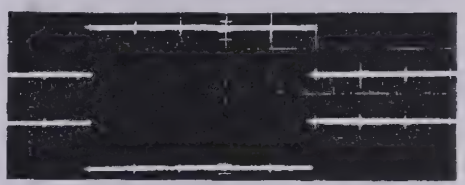
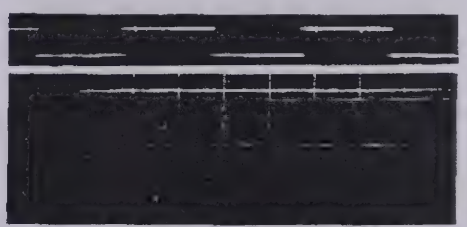
(4) Although only the key test points are available at the top of the printed-circuit card assemblies, many other waveforms and measurements can be obtained by using the extender card supplied with the vlf-12B accessory kit. Be sure to use the special card extractor every time a module is removed for testing or service.

*c. Signal Substitution and Gain Measurement.*

(1) Troubleshooting of the RF and IF modules can be accomplished by injecting a signal of known frequency and amplitude into the antenna input. An excellent signal source is available from the rear panel BNC connector that provides a corrected 10-kc output. To prevent overloading the vlf-12B, insert a step attenuator in the coaxial line to obtain an input signal magnitude of 1 millivolt peak-to-peak or 0.35 millivolt rms. Access to RF module test points is obtained by removing the module; access is obtained through use of the standard printed-circuit card extender.

(2) Remove module A2 and insert a 10,000-ohm resistor as a dummy load between pin 23a of module A1 and ground. Adjust the DB ATTENUATION switch on the front panel to 0 db before making the waveform and gain measurements. The frequency of the signal waveform before the mixer stage is 10.0 kc; after the mixer stage, the waveform frequency is 12.25 kc. The gain throughout the stages varies; however, the overall gain from

## TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART

| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| | NORMAL MODE 2ND MIXER | | Time Base 20 usec/cm<br>Vertical Amp. 2.0 v/cm<br>Sync Int |
| A4 | | TP1 |  |
| A4 | " | TP2 | |
| | | | Time Base 50 usec/cm<br>Vertical Amp 5v/cm<br>Sync Ext @ A5-TP8 |
| A5 | 3 FLIP-FLOPS AND GATES | TP1 |  |
| A5 | " | TP2 | |
| A5 | " | TP3 |  |
| A5 | " | TP4 | |
| | | | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A5 | " | TP5 |  |
| A5 | " | TP6 | |
| | | | Time Base 5ms/cm TP-7, 5 usec/cm TP-8<br>Vertical Amp 2.0v/cm TP-7, 2v/cm TP-8<br>Sync Ext @ A5-TP8 |
| A5 | " | TP7 |  |
| A5 | " | TP8 | |

## TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

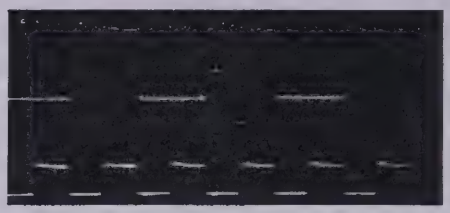
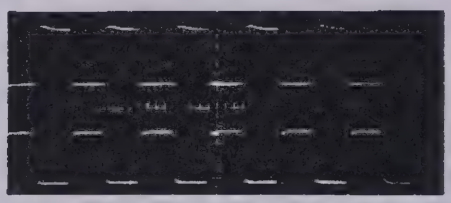
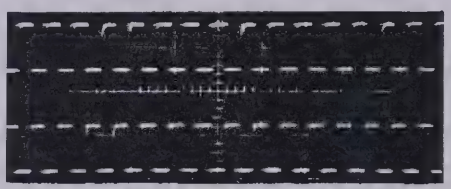
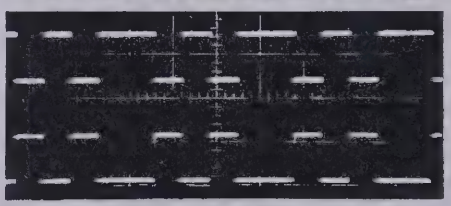
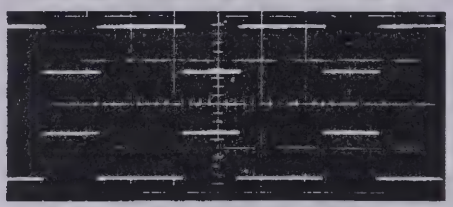
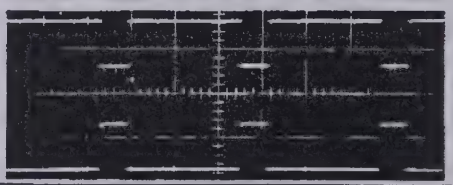
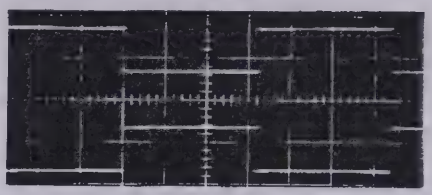
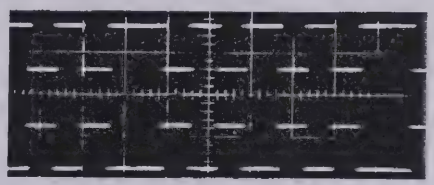
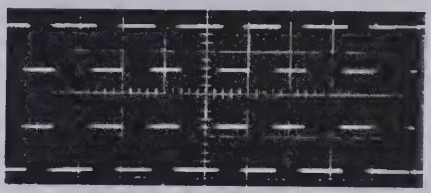
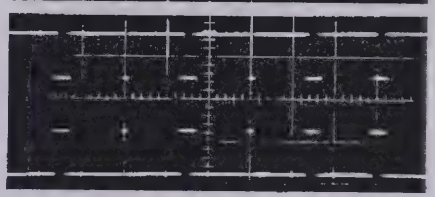
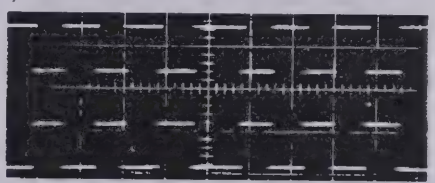
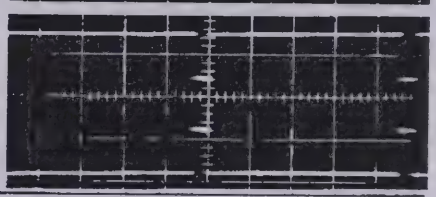
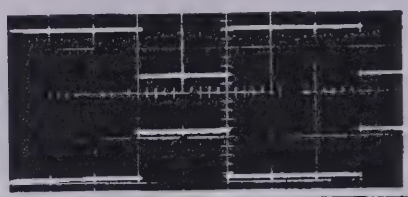
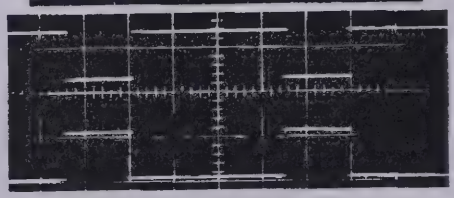
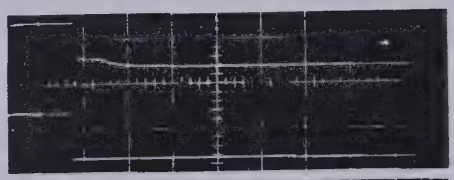
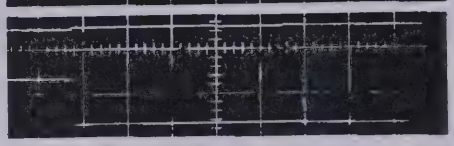
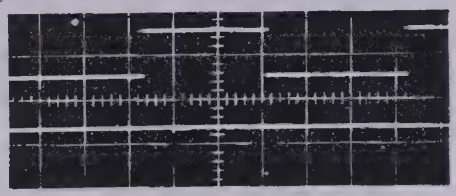
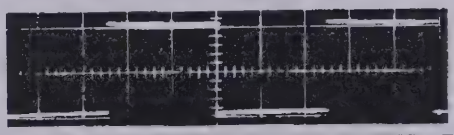
| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| | | | Time Base 10 usec/cm (Set Channel Selector 19kc)<br>Verical Amp 10v/cm<br>Sync Ext @ A5-TP8 |
| A6 | LOCAL OSCILLATOR AND VCO | TP1 |  |
| A6 | " | TP2 | |
| | | | Time Base 10 usec/cm (Set Channel Selector 19kc)<br>Vertical Amp 5v/cm<br>Sync Ext @ A5-TP8 |
| A6 | " | TP2 |  |
| A6 | " | TP3 | |
| | | | Time Base 50 usec/cm<br>Vertical Amp 5v/cm<br>Sync Ext @ A5-TP8 |
| A7 | MOD-10 (UNITS DIVIDER) | TP1 |  |
| A7 | " | TP2 | |
| A7 | " | TP3 |  |
| A7 | " | TP4 | |
| A7 | " | TP5 |  |
| A7 | " | TP6 | |
| A7 | " | TP7 |  |
| A7 | " | TP8 | |

TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| | | | Time Base 50 usec/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A8 | MOD-10 (UNITS DIVIDER) | TP1 |  |
| A8 | " | TP2 | |
| | | | Time Base 5 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A8 | " | TP3 |  |
| A8 | " | TP4 | |
| | | | Time Base 0.5ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A8 | " | TP5 |  |
| A8 | " | TP6 | |
| A8 | " | TP7 |  |
| A8 | " | TP8 | |
| | | | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A9 | FOUR FLIP-FLOPS (HUNDREDS DIVIDER) | TP1 |  |
| A9 | " | TP2 | |
| A9 | " | TP3 |  |
| A9 | " | TP4 | |

## TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| | | | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A9 | FOUR FLIP-FLOPS (HUNDREDS DIVIDER) (cont) | TP5 |  |
| A9 | " | TP6 | |
| A9 | " | TP7 |  |
| A9 | " | TP8 | |
| | | | Time Base 5 usec/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A10 | ONE-SHOT AND RESET | TP1 |  |
| A10 | " | TP2 | |
| A10 | " | TP3 |  |
| A10 | " | TP4 | |
| | | | Time Base 0.5ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A5-TP8 |
| A10 | " | TP5 |  |
| A10 | " | TP6 | |
| | | | Time Base 2 ms/cm<br>Vertical Amp 1 v/cm<br>Sync Ext @ A5-TP8 |
| A12 | SYNTHESIZER PHASE DETECTOR (SLOW-LOOP) | TP1 |  |

## TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

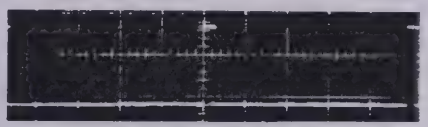
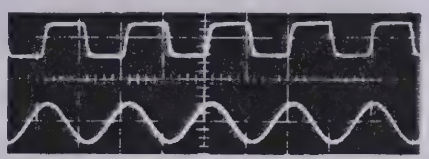
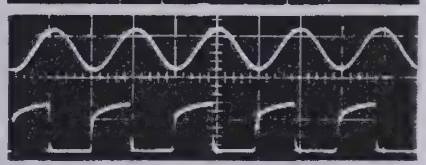
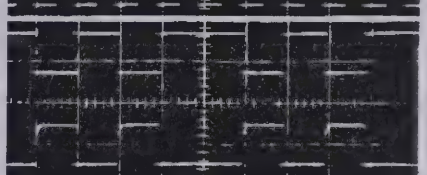
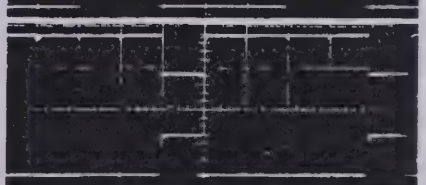
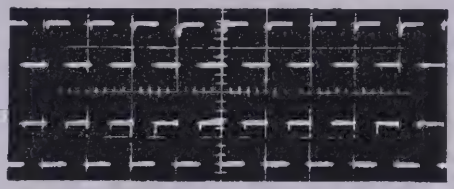
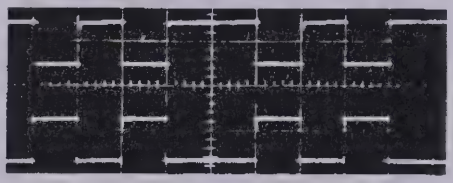
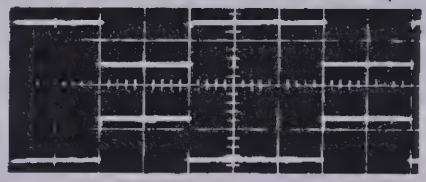
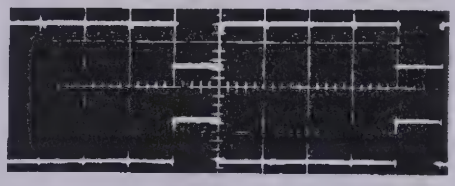
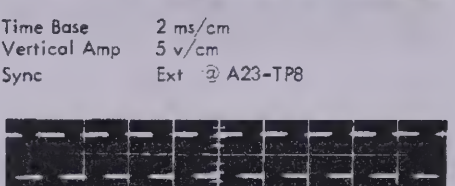
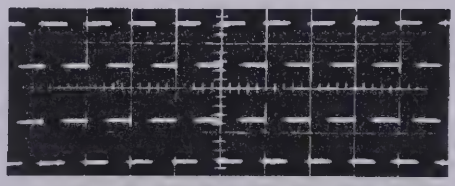
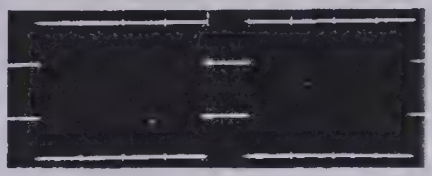
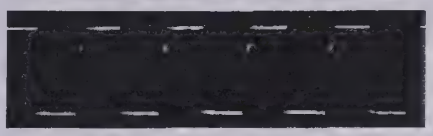
| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| A13 | SYNTHESIZER PHASE DETECTOR (FAST LOOP) | TP1 | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A7-TP3 (TP1), A3-TP2 (TP2)<br>  |
| A13 | " | TP2 | |
| A14 | 100KC AMPLIFIER AND PHASE SHIFTER | TP1 | Time Base 5 usec/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A14-TP4<br>  |
| A14 | " | TP2 | |
| A14 | " | TP3 |  |
| A14 | " | TP4 | |
| A21 | MOD-10 100 KC TO 10 KC DIVIDER | TP1 | Time Base 20 usec/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A23-TP8<br> |
| A21 | " | TP2 | |
| A21 | " | TP3 |  |
| A21 | " | TP4 | |
| A21 | " | TP5 | |
| A21 | " | TP6 | |
| A21 | " | TP7 |  |
| A21 | " | TP8 | |

TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| | | | Time Base 0.2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A23-TP8 |
| A22 | MOD-10 10KC TO 1 KC DIVIDER | TP1 |  |
| A22 | " | TP2 |  |
| A22 | " | TP3 |  |
| A22 | " | TP4 |  |
| A22 | " | TP5 |  |
| A22 | " | TP6 | |
| A22 | " | TP7 | |
| A22 | " | TP8 | |
| | | | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A23-TP8 |
| A23 | MOD-10 1 KC TO 100 PPS DIVIDER | TP1 |  |
| A23 | " | TP2 | |
| A23 | " | TP3 | |
| A23 | " | TP4 | |

## TABLE 4-2. WAVEFORM TROUBLE ANALYSIS CHART (Cont)

| REF DES | MODULE | TEST POINT | WAVE FORM |
|---|---|---|---|
| A23 | MOD-10 .1 KC TO 100 PPS DIVIDER (cont) | TP5 | Time Base 2 ms/cm<br>Vertical Amp 5 v/cm<br>Sync Ext @ A23-TP8<br> |
| A23 | " | TP6 |  |
| A23 | " | TP7 | |
| A23 | " | TP8 | |
| A25 | OUTPUT BUFFERS | TP1 | Time Base 50 usec/cm (TP1), 5usec/cm (TP2)<br>Vertical Amp 1 v/cm<br>Sync Ext @ A23-TP8<br> |
| A25 | " | TP2 |  |
| A25 | " | TP3 | Time Base 5ms/cm (TP3), 0.5ms/cm (TP4)<br>Vertical Amp 1 v/cm<br>Sync Ext @ A23-TP8<br> |
| A25 | " | TP4 | |
| A1 | RF AMP & 1ST MIXER | NONE | |
| A2 | IF, & AGC AMPLIFIERS | NONE | |
| A3 | X4 MULTIPLIER | TP1,2,& 3 | Amplitude Varies with Attenuator Setting (For alignment only) |
| A15 | SERVO & AGC PHASE DETECTOR | NONE | |
| A16 | 1KC IF AMP | TP1 & 2 | |
| A17 | SERVO CUTOUT | NONE | |
| A18 | SERVO MOTOR DRIVE | TP1 & 2 | DC Error Signal Chopped at Approx 1 kc |
| | " | TP3 & 4 | DC Error Signal |
| A19 | AUDIO AMPLIFIER | TP1 | Approx 1 kc Audio (Code) |
| A20 | ±12V POWER SUPPLY | TP1 | Zero (Ground) |
| | | TP2 | -12 V DC |
| | | TP3 | -12 V DC |
| | | TP4 | Zero (Ground |

the antenna input to the output at pin 23a of module A1 should be approximately 55 db, when measured with a Hewlett-Packard model 400D ac vacuum-tube voltmeter or equivalent.

(3) Utilizing the same setup given in paragraph 4–6*c*(1) above, observe the waveforms and measure the gain of IF amplifier module A2. Remove the dummy load inserted in paragraph 4–6*c*(2) and re-insert module A2. Then remove servo and agc phase detector module A15, and connect a jumper across C13 on the IF amplifier card to remove the agc voltage. The waveform throughout the IF amplifier card is sinusoidal, with a frequency of 12.25 kc. The overall gain from pin 7H to pin 18V is approximately 75 db without agc. This represents a voltage gain of approximately 10,000. In order to prevent overloading of the final stage, the DB ATTENUATION switch must be used to decrease the input voltage at pin 2B to approximately 100 millivolts peak-to-peak.

(4) The second IF stage (module A16) can also be tested in a similar manner. This module consists basically of two separate 1-kc IF sections. The first section is composed of Q1 through Q3, and is used to provide a 1-kc carrier monitor from a BNC connector on the rear panel. This output is used for time "ticks" and as an audio output. The Q1–Q3 section produces a gain of approximately 30 db. The second section, consisting of Q4 through Q11, exhibits a bandwidth of 50 cps, and is used for vlf tracking operations. The gain of the second section is approximately 32 db. In order to measure the gain of this stage, perform the following steps:

(*a*) Remove module A4.

(*b*) Using an audio signal generator (Hewlett-Packard model 200CD), connect a signal whose amplitude is approximately 10 millivolts to pin 4D.

(*c*) Using an oscilloscope (Tektronix model 561A) or an ac vacuum-tube voltmeter (Hewlett-Packard model 400D), measure the gain of the first section at pin 10L.

(*d*) Disconnect the audio signal generator output from pin 4D, and connect it to pin 14R.

(*e*) Using an oscilloscope or ac vacuum-tube voltmeter, measure the gain of the second section at pin 23a.

(5) Slight variations of 1 or 2 decibels in the gain measurements do not indicate a malfunction. However, variations greater than this do indicate that a stage is not operating properly. In this case, further checks should be made to determine which component or components may be defective.

*d. 76.8- to 100-KC Converter (A24) Troubleshooting Instructions.*

(1) Failure of the 76.8-kc to 100-kc converter may be suspected by failure of the vlf-12B to track when the INTERRUPT WARNING light remains out. This can be verified by switching the front panel METER FUNCTION switch to the 100KC or 100PPS position. If the meter fails to read in the green area when in the 100KC position and the INTERRUPT WARNING light remains out, a square converter card should be substituted. It should be noted, however, that if the INTERRUPT WARNING light is on, it is probable that the 76.8-kc to 100-kc converter is functioning properly, but that the local frequency standard or the 100-kc amplifier and phase shifter card has failed. Moreover, if in the 100KC position of the METER FUNCTION switch the meter reads properly, but in the 100PPS position it does not read in the green, then the trouble can exist elsewhere, but not in the 76.8-kc to 100-kc converter.

(2) An oscilloscope such as the Tektronix model 561A should be used to check the waveform and frequency of TP1 of the A24 (76.8-kc to 100-kc converter) card. The waveform should be a square wave of approximately 6 volts peak-to-peak, and have transition times of less than 1 microsecond. The frequency should be exactly 384 kc (depending on the accuracy of the local standard). Failure of the input X5 multiplier will cause the signal at TP1 to vary from these conditions. If these conditions are met, failure has occurred farther down the divider chain. The following test points should be tested in the same manner, and should give the indicated results:

TP2 Square wave 1 μsec transition times 64 kc
TP3 Square wave 1 μsec transition times 320 kc
TP4 Square wave 1 μsec transition times 80 kc
TP5 Square wave 1 μsec transition times 400 kc
TP6 Square wave 1 μsec transition times 100 kc

(3) If the signal to TP6 is normal, then failure has occurred elsewhere. The trouble can then be localized by continuing to check several test points in the reference divider chain.

*e. Malfunction Isolation Within a Model*

(1) If facilities are available for the repair of individual card assemblies, the following paragraphs provide useful information for isolating a malfunction to a specific components. When isolating malfunctions within a module, the extender card is used. The length of the signal and ground leads is increased, and the shielding by the card assembly "bucket" is not available to the card on the extender. In this case, some cards with high-gain circuits may exhibit shortly varying characteristics that do not exist when the card is inserted into its appropriate connector in the "bucket." Such occurrences are normal, and should be ignored during troubleshooting.

(2) Always make a visual inspection of the card assembly under test to first determine whether there are any burned components or poor solder joints. Such obvious faults can be found without extensive troubleshooting.

(3) Observe the input and output waveform of each stage within a module. The waveshapes of some modules have little or no meaning; this is especially true in the servo section, where error signals appear as dc levels. Some experience in troubleshooting is required in order to determine exactly what is expected at each circuit. It is also important that maintenance personnel be thoroughly familiar with the theory of operation.

(4) In those stages where the waveshapes have little or no meaning, voltage measurements are helpful. The voltage levels at the base, collector, and emitter of a transistor are often helpful in determining which stage is defective, and also quite often helpful in determining a malfunctioning component. Always use a vacuum-tube voltmeter with a high input impedance, since a meter with a low internal impedance would tend to load the circuit and thus produce erroneous results.

(5) An open or shorted transistor can be located by making resistance measurements at the junctions of the transistor. A normal transistor displays a high resistance in one direction and a low resistance when the ohmmeter leads are reversed. The exact value of base-to-emitter, base-to-collector, or emitter-to-collector resistance varies with the different transistor types. However, a short or open circuit can easily be detected with this procedure.

***Caution:*** **Ascertain that the input power is disconnected and that the module is removed from the vlf-12B when making resistance measurements. Check the circuit schematic to determine whether resistors or other components are shunting the transistor, thus producing erroneous indications. If other components are shunting the transistor, it is necessary to disconnect one of the junctions of that component before the proper resistance measurement can be obtained.**

(6) A transistor with low $H_{fe}$ or high $I_{cbo}$ can be found only by removing the transistor from the printed-circuit card and using a transistor checker to test its parameters. Transistors that display characteristics exceeding the manufacturer's specification by more than 10 percent should be replaced.

## 4–7. Removal and Replacement

*a. General.* When component parts are replaced on the printed-circuit cards, exercise care to avoid damaging other components on the card. Before removing a part, the card should be placed in a simple card holder that is designed to allow access to all parts of the card, and yet securely hold the card. Parts may then be removed and replaced as directed in the following steps. Additional instructions are provided in TB SIG 222.

(1) Use the TL–705/U soldering iron to melt the solder at one joint of the component being removed. Do not apply more heat than is necessary to melt the solder. At the same time, use a syringe with a teflon tip to remove the melted solder at the joint.

(2) Use a sharp knife or similar tool to pick up the bent lead from the joint where the solder is removed.

(3) On the opposite side of the card, use a pair of needle-nose pliers to grip the lead of

the component to be removed. Exert a slight even pull while simultaneously using a soldering iron to heat the joint on the other side. Repeat this procedure for all leads on the component until it can be removed.

(4) Be sure that all excess solder is removed from the holes in the printed-circuit card before replacing the component.

(5) Bend the leads of the replacement components until they are aligned with the holes in the printed-circuit card; then carefully insert the component.

(6) Bend over the leads on the opposite side of the printed-circuit card, and use a pair of diagonal cutters to clip off the excess leads.

(7) Use a heat sink (para 4–5*d*) when replacing transistors and diodes, to prevent possible damage to these devices.

*b. Replacement of Factory-Selected Components.* The following assemblies contain components that are factory-selected: IF and agc amplifiers, A2; normal-mode second mixer, A4; 100-kc amplifiers and phase shifter, A14; 1-kc IF amplifier, A16; and the ±12-volt power supply, A20. If replacement of factory-selected components becomes necessary, perform the following value selection procedure:

(1) *IF and agc amplifiers, A2.* Resistor R34 (fig. 3–12) is used to calibrate the front-panel meter for carrier indication. The value range of the resistors used should be 330 ohms to 620 ohms in increments of 30 ohms to 60 ohms with a nominal value of 390 ohms.

(*a*) Turn METER FUNCTION switch to CARRIER.

(*b*) Substitute resistors, starting with the nominal value (390 ohms), until the front-panel meter reads in the green area and the CARRIER lamp is off.

(2) *Normal-mode second mixer, A4.* The value of capacitor C3 (fig. 3–13) establishes the resonant point of the 45-kc tank circuit of L1 and C3. The value range of the capacitors used should be 250 pf to 620 pf in increments of 20 pf to 40 pf with a nominal value of 430 pf.

(*a*) Connect the oscilloscope to TP1 and adjust to obtain waveform shown in table 4–2.

(*b*) Substitute capacitors, starting with the nominal value (430 pf), until correct output is obtained.

(3) *100-kc amplifier and phase amplifier, A14.* Resistor R24 (fig. 3–27) is used to calibrate the front-panel meter for 100-kc indication. The resistor values used are 110K, 120K, and 130K (nominal value).

(*a*) Turn METER FUNCTION switch to 100 KC.

(*b*) Substitute resistors, starting with the nominal value (130K), until the front-panel meter reads in the center of the green area.

(4) *1-kc amplifier, A16.* The value of capacitor C10 (fig. 3–22) establishes the resonant point of the 1-kc tank circuit of L2, C8, and C10. The value range of the capacitors should be 1200 pf to 2700 pf in increments of 100 pf to 200 pf with a nominal value of 1800 pf.

(*a*) Connect oscilloscope to TP1.

(*b*) Substitute capacitors, starting with the nominal value (1800 pf), until maximum 1-kc signal is obtained on oscilloscope.

(5) *±12-volt power supply.* The value of resistor R4 (fig. 3–25) controls the threshold bias of current-limiting transistor Q2. The value range of the resistors used should be 1K to 3K in increments of 100 ohms to 300 ohms with a nominal value of 2K.

(*a*) Turn METER FUNCTION switch to +12V.

(*b*) Substitute resistors, starting with the nominal value (2K), until the reading on the front-panel meter starts to drop.

(*c*) Select as the replacement for R4 the resistor substituted just before the meter reading started to drop.

*c. Removable Assemblies.* Procedures are given for the removal of the following assemblies:

(1) Chart recorder.

(2) Servo assembly (A27), which includes the servo motor, MICROSECONDS counter, precision potentiometer, phase shifter, and associated gear train.

(3) Digital thumbwheel switches (A28).

(4) DC-to-dc converter.

(5) SERVO selector switch (S8).

(6) METER FUNCTION switch (S7).

(7) RF module (A1).

*Note.* With the exception of the servo assembly, it is recommended that all other components be replaced as a complete unit. The chart recorder should be returned to higher echelon for repairs.

*d. Preliminary Instructions.* In order to remove and replace the assemblies listed in paragraph 4–7*b*, it is first necessary to remove the vlf-12B from the cabinet, and then proceed as follows:

(1) Open the rear door of bay 2 (unit 2), and proceed as follows:

(*a*) Remove the power cord from the ac receptacle.

(*b*) Disconnect the antenna triaxial cable from the antenna 50-ohm receptacle (J1).

(*c*) Disconnect the coaxial cable from the LOCAL STD input receptacle (J3).

(2) Open the front door of bay 2 (unit 2), and remove the four panel screws and cup washers which secure the vlf-12B to the cabinet frame.

(3) Carefully withdraw the vlf-12B on its chassis rails until the mechanical limit stops are reached; then release the catches on each chassis rail and remove the vlf-12B from the chassis rails.

*e. Chart Recorder.* The following steps supply the instructions for removal and replacement of the chart recorder:

(1) Remove the top and bottom covers of the vlf-12B.

(2) Disconnect the plug at the rear of the recorder.

(3) At the top of the recorder, remove the two recorder retaining screws.

(4) Open the front panel of the recorder and remove the two screws from the bottom of the recorder.

(5) Withdraw the recorder from the front panel of the vlf-12B.

(6) Reverse the procedure of steps (1) through (5) to replace the recorder.

*f. Servo Assembly (A27).* The following steps should be utilized for removal and installation of the servo assembly:

(1) Remove the chart recorder (para 4–7*d*).

(2) Remove the two screws that hold the cover plate to the servo motor, and unsolder the two motor leads.

(3) Remove the three screws that hold the top cover of the servo assembly, and unsolder the red, purple, and white leads (from the solder terminals near the front of the assembly) leading to the potentiometer. Also unsolder the three coaxial leads from the phase shifter.

*Note.* When unsoldering leads from any assembly, use identification tags on the leads to assist in attaching the leads to the same assemblies from which they were removed.

(4) Remove the knob and SERVO switch assembly.

(5) On the front panel studs, remove the four nuts that hold the assembly in place.

(6) Remove the servo assembly from the top of the vlf-12B.

*Note.* When the servo assembly is removed from the receiver, the servo motor, phase shifter, and precision potentiometer can be removed.

(7) Remove the servo motor as follows:

(*a*) Loosen the two setscrews on the motor-shaft coupling.

(*b*) Remove the two screws that hold the motor to the servo assembly body.

(*c*) Withdraw the servo motor.

(*d*) Replace the servo motor by reversing steps (*a*) through (*c*).

(8) Remove the phase shifter as follows:

(*a*) Loosen the setscrew on the shaft coupling.

(*b*) Remove the three screws that hold the phase shifter to the servo assembly body.

(*c*) Withdraw the phase shifter.

(*d*) Replace the phase shifter by reversing steps (*a*) through (*c*).

(9) Remove the precision potentiometer as follows:

(*a*) Loosen the setscrew on the shaft coupling.

(*b*) Unsolder the three potentiometer leads.

(*c*) Loosen the two screws that hold the potentiometer to the servo body.

(*d*) Withdraw the precision potentiometer.

(*e*) Replace the precision potentiometer by reversing steps (*a*) through (*d*).

(10) To replace the servo assembly, reverse steps (1) through (9) above.

*g. Digital Thumbwheel Switch.* The following steps provide the procedure for removal and replacement of the digital thumbwheel switch.

(1) Remove the top and bottom covers of the vlf-12B.

(2) Remove the four screws and lock washers that hold the handles to the front panel assembly.

(3) Loosen the two setscrews that hold the attenuator shaft to RF assembly A1A1; disengage the coupling from the shaft of switch A1S1.

(4) Open the front panel of the recorder and remove the two screws from the bottom of the recorder.

(5) On the front panel studs, remove the four nuts that hold the switch in place.

(6) Unsolder and tag all leads to the thumbwheel switch.

(7) Tilt the front panel of the receiver forward, and remove the thumbwheel switch from the panel assembly.

(8) To replace the digital thumbwheel switch, reverse the procedure of steps (1) through (7).

*h. DC-to-DC Converter.* The following steps provide the procedure for removal and installation of the dc converter.

(1) Remove the top and bottom covers of the vlf-12B. On the rear panel, remove the four screws that hold the line filter (FL1). With all leads intact, lay the line filter aside to gain access to the connections on the dc converter.

(2) Unsolder and tag leads to the fuseholder; then remove the fuseholder.

(3) Unsolder and tag all leads to the dc converter.

(4) Remove the four screws that secure the dc converter to the chassis.

(5) Withdraw the dc converter from the top of the vlf-12B.

(6) To replace the dc converter, reverse the procedures of steps (1) through (5).

*i. Servo (S8) and Meter Function (S7) Switches.* The following procedures can be utilized to remove and replace the SERVO and METER FUNCTION selector switches:

(1) Unsolder and tag all leads to the switch.

(2) On the front panel, remove the switch control knob.

(3) Remove the hexagonal nut that secures the switch to the front panel.

(4) Withdraw the switch from the rear of the front panel.

(5) Replace the switch by reversing the procedure of steps (1) through (4).

*j. RF Module (A1).* The following steps provide the procedure for removal and replacement of RF module A1:

(1) Loosen the two setscrews on the coupling shaft of the attenuator.

(2) Remove the four screws that secure module A1 to the rear panel.

(3) Pull straight up to remove the entire module from it connector.

(4) Replace RF module A1 by reversing the procedure of steps (1) through (3).

## 4-8. Alignment and Calibration Procedures

*a. General.* The vlf-12B is completely aligned and calibrated at the factory. No further alignment is required to place the unit in operation. When repairs are made to the unit by removing components from the printed-circuit cards, replacement parts should be of the same type to ensure that the designed accuracy and precision of the equipment are retained. When components of the tank circuits are replaced, they must be hand-selected to achieve the proper frequency and bandpass characteristics of the circuit. The only adjustments that may be necessary are on the synthesizer phase detector "slow-loop" (module A12), servo and agc phase detectors (module A15), servo cutout (module A17), and ±12-volt power supply (module A20). The adjustments on these cards are necessary only if repair is performed that would affect the circuit.

*b. Synthesizer Phase Detector, Slow-Loop (A12).* This adjustment to the synthesizer phase detector "slow-loop" (module A12)

sets the proper voltage to the voltage-controlled oscillator.

(1) Remove module A12 and insert the extender card.

(2) Insert module A12 into the extender-card socket. Then use a jumper wire to short C4; this eliminates the phase loop.

(3) Operate the CHANNEL SELECTOR switch to 19.0 kc.

(4) Apply power to the vlf-12B.

(5) Use an oscilloscope (Tektronix model 535A or equivalent) to observe the waveform at TP1. The waveform should be a 100-cps square wave with a 100-pps pulse superimposed on it.

(6) Adjust R22 on module A12 until the 100-pps pulse coincides with the trailing edge of the square wave.

(7) Disconnect the oscilloscope, remove the jumper from C4, and remove the power from the vlf-12B.

(8) Re-insert module A12.

*c. Servo and AGC Phase Detector (A15).* This adjustment to the servo and agc phase detector (module A15) is the phase detector balance.

(1) Remove the 12.25-kc IF amplifier (module A2). This removes the signal to the phase detector, thus reducing noise.

(2) Apply power to the vlf-12B.

(3) Operate the METER FUNCTION selector switch to the PHASE position.

(4) Adjust variable resistor R11 on module A15 until the front-panel meter indicates in the green band.

*Note.* Since there is a long time constant associated with this circuit, it is necessary to wait one or two minutes after adjusting R11, and then readjust as required to maintain the meter indication in the green band.

(5) Remove power to the vlf-12B.

(6) Replace module A2.

*d. Servo Cutout (A17).* This adjustment to the servo cutout (module A17) is made to set the carrier threshold level at which the servo will disconnect. The normal procedure is to have the relay disconnect the servo when the antenna input falls below 0.003 microvolt, and reconnect when the input goes above 0.01 microvolt. The difference is caused by the hysteresis in the relay circuit. A coherent signal at the antenna is required to perform this adjustment. A coherent signal generator may be used, or the 10-kc coherent output from the rear of the vlf-12B.

(1) Apply power to the vlf-12B.

(2) Use one of the two methods suggested above, and connect a coherent signal to the 50-ohm antenna input on the rear panel.

(3) If the 10-kc coherent signal from the rear of the vlf-12B is used, the signal level must be measured by utilizing a calibrated oscilloscope (Tektronix model 561A or equivalent).

(4) When the exact voltage of the 10-kc coherent signal is determined, use a step attenuator of sufficient attenuation to reduce the input at the antenna connector to voltages ranging from 0.003 to 0.01 microvolt.

(5) Operate the CHANNEL SELECTOR switch to 10.0 kc.

(6) Adjust variable resistor R7 on module A17 until the CARRIER/PWR STD indicator energizes as the voltage goes below 0.003 microvolt, and deenergizes when the voltage rises above 0.01 microvolt.

(7) Disconnect the coherent signal input to the antenna.

(8) Remove power to the vlf-12B.

*e. Plus and Minus 12-volt Power Supply (A20).* These adjustments to the ±12-volt power supply (module A20) set the vlf-12B voltages at plus and minus 12 volts.

(1) Apply power to the vlf-12B.

(2) Connect the positive probe of a dc voltmeter (Hewlett-Packard model 410B or equivalent) to TP2 of module A20. Connect the negative probe to TP1 (ground).

(3) Adjust variable resistor R15 on module A20 until the dc voltmeter indicates +12 vdc.

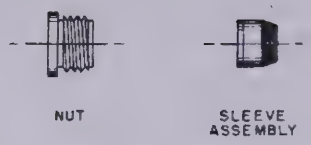
(4) Remove the positive probe from TP2.

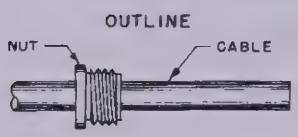
(5) Operate the dc voltmeter for negative voltage measurements.

(6) Connect the positive probe to TP3 of module A20; then connect the negative probe to TP4.

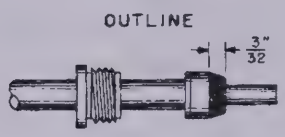
(7) Adjust variable resistor R17 on module A20 until the dc voltmeter indicates −12 vdc.

(8) Remove both probes, and then remove the power from the vlf-12B.

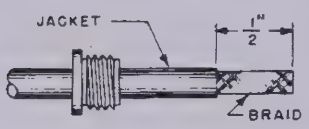




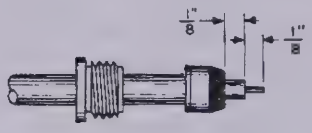

1. CUT OFF SHARP.



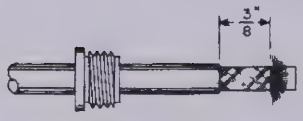

6. WITH SLEEVE IN PLACE, COMB OUT BRAID, FOLD BACK SMOOTH AS SHOWN, AND TRIM TO $\frac{3}{32}$ INCH FROM END.



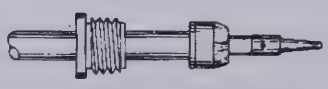

2. CUT OFF JACKET $\frac{1}{2}$ INCH FROM END. BE CAREFUL NOT TO NICK BRAID.




7. CUT INNER DIELECTRIC $\frac{1}{8}$ INCH FROM BRAID. BE CAREFUL NOT TO NICK INNER CONDUCTOR. CUT OFF INNER CONDUCTOR $\frac{1}{8}$ INCH FROM END OF DIELECTRIC.

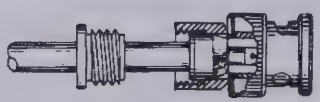



3. CUT OFF INNER INSULATION AND WIRE UNDER BRAID $\frac{3}{8}$ INCH FROM END OF JACKET.

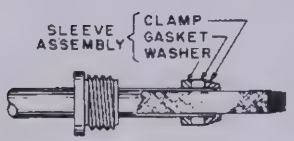


8 TIN INSIDE HOLE OF MALE CONTACT, TIN CENTER CONDUCTOR OF CABLE, SLIP MALE CONTACT IN PLACE AND SOLDER, REMOVE EXCESS SOLDER. BE SURE CABLE DIELECTRIC IS NOT HEATED EXCESSIVELY AND SWOLLEN SO AS TO PREVENT DIELECTRIC ENTERING BODY.

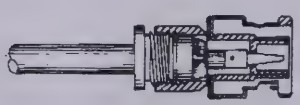
4. TAPER BRAID.



9. PUSH INTO BODY AS FAR AS IT WILL GO, THEN SLIDE NUT INTO BODY AND SCREW INTO PLACE, WITH WRENCH UNTIL MODERATELY TIGHT. HOLD CABLE AND SHELL RIGIDLY AND ROTATE NUT.




5. SLIDE SLEEVE OVER TAPERED BRAID TO FIT TIGHT AGAINST JACKET. BE SURE INNER SHOULDER OF SLEEVE FITS SQUARELY AGAINST END OF CABLE JACKET.

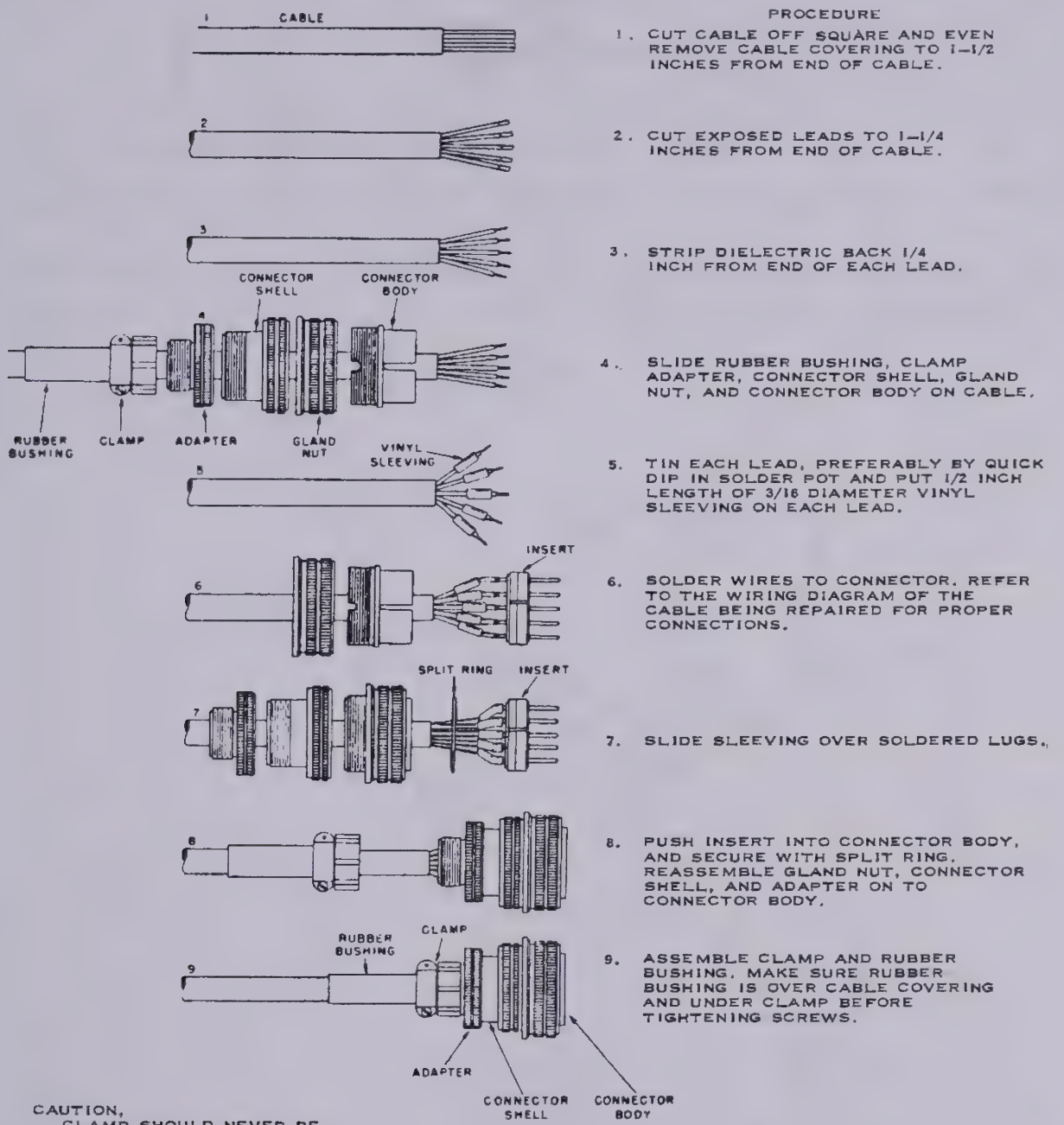


FINAL ASSEMBLY SHOWN IN CROSS SECTION

EL5895-413-15/3-36.

*Figure 4-1. Coaxial cable repair*

STEPS 1 THROUGH 9 BELOW ARE USED WHEN REPLACING A CABLE CONNECTOR. WHEN THE REPAIR OF A BROKEN LEAD IS NEEDED, OMIT STEPS 1 THROUGH 3, AND PROCEEDE WITH STEP 4 EXCEPT THAT IT MAY NOT BE NECESSARY TO SEPARATE THE CONNECTOR BODY FROM THE INSERT (STEP 6).




PROCEDURE

1. CUT CABLE OFF SQUARE AND EVEN REMOVE CABLE COVERING TO 1-1/2 INCHES FROM END OF CABLE.
2. CUT EXPOSED LEADS TO 1-1/4 INCHES FROM END OF CABLE.
3. STRIP DIELECTRIC BACK 1/4 INCH FROM END OF EACH LEAD.
4. SLIDE RUBBER BUSHING, CLAMP ADAPTER, CONNECTOR SHELL, GLAND NUT, AND CONNECTOR BODY ON CABLE.
5. TIN EACH LEAD, PREFERABLY BY QUICK DIP IN SOLDER POT AND PUT 1/2 INCH LENGTH OF 3/16 DIAMETER VINYL SLEEVING ON EACH LEAD.
6. SOLDER WIRES TO CONNECTOR. REFER TO THE WIRING DIAGRAM OF THE CABLE BEING REPAIRED FOR PROPER CONNECTIONS.
7. SLIDE SLEEVING OVER SOLDERED LUGS.
8. PUSH INSERT INTO CONNECTOR BODY, AND SECURE WITH SPLIT RING. REASSEMBLE GLAND NUT, CONNECTOR SHELL, AND ADAPTER ON TO CONNECTOR BODY.
9. ASSEMBLE CLAMP AND RUBBER BUSHING. MAKE SURE RUBBER BUSHING IS OVER CABLE COVERING AND UNDER CLAMP BEFORE TIGHTENING SCREWS.

CAUTION,
CLAMP SHOULD NEVER BE TIGHTENED ON WIRES STRIPPED OF CABLE COVERING.

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*Figure 4-2. Multiconductor cable repair*

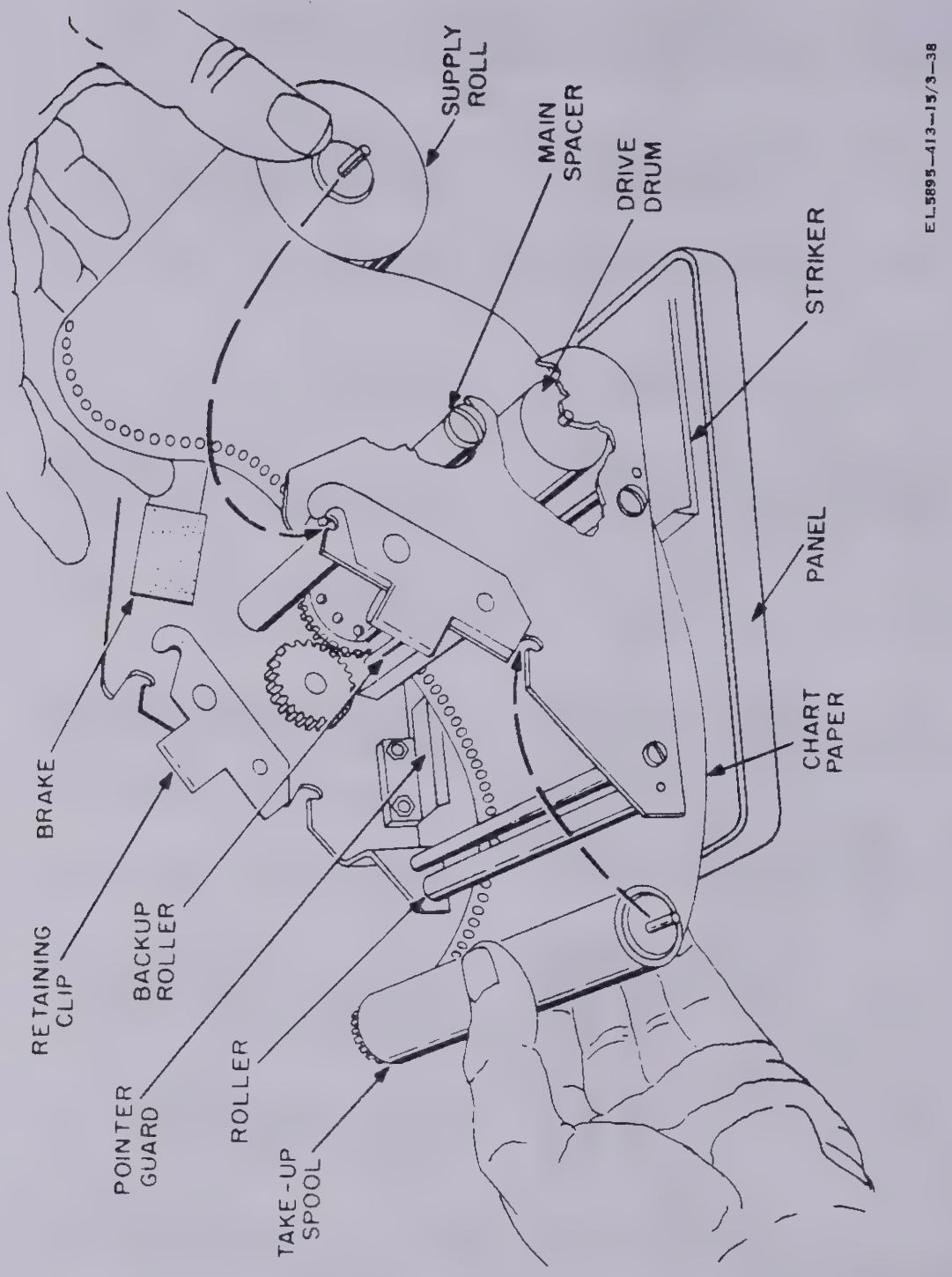


*Figure 4–3. Loading chart recorder*

# CHAPTER 5

# ILLUSTRATIONS

## 5-1. Illustrations in Part III (TM 11-5895-413-15/3)

The illustrations in this manual include block diagrams, schematic diagrams, and parts placement illustrations. A list of illustrations is provided in the front of this manual.

## 5-2. Illustrations in Part I (TM 11-5895-413-15/1) and Part II (TM-11-5895-413-15/2)

Illustrations for the station timing units are contained in TM 11-5895-413-14/1 (Part I) and in TM 11-5895-413-14/2 (Part II).

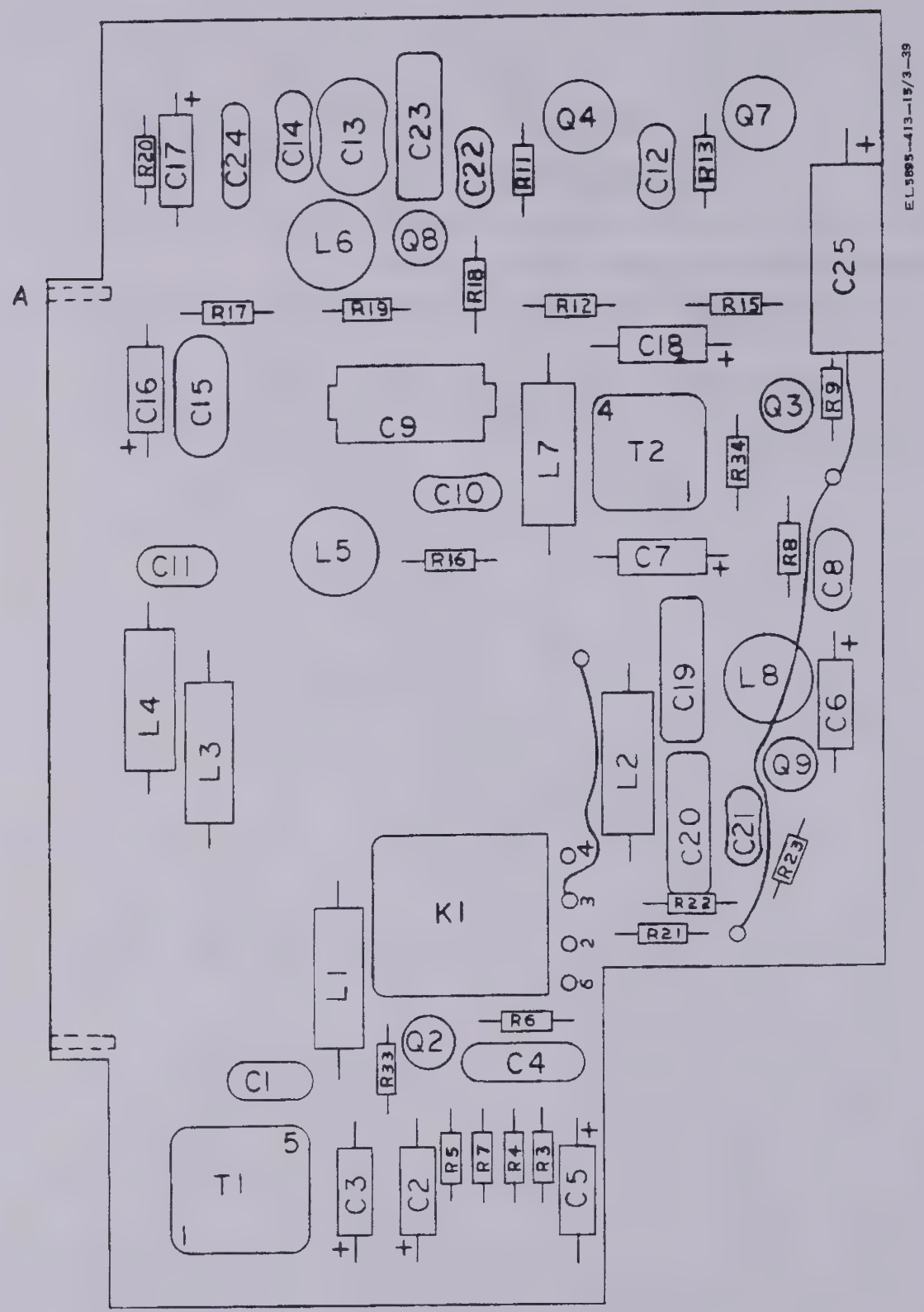


*Figure 5-1. RF amplifier and first mixer assembly, A1A1 (part No. 200180).*

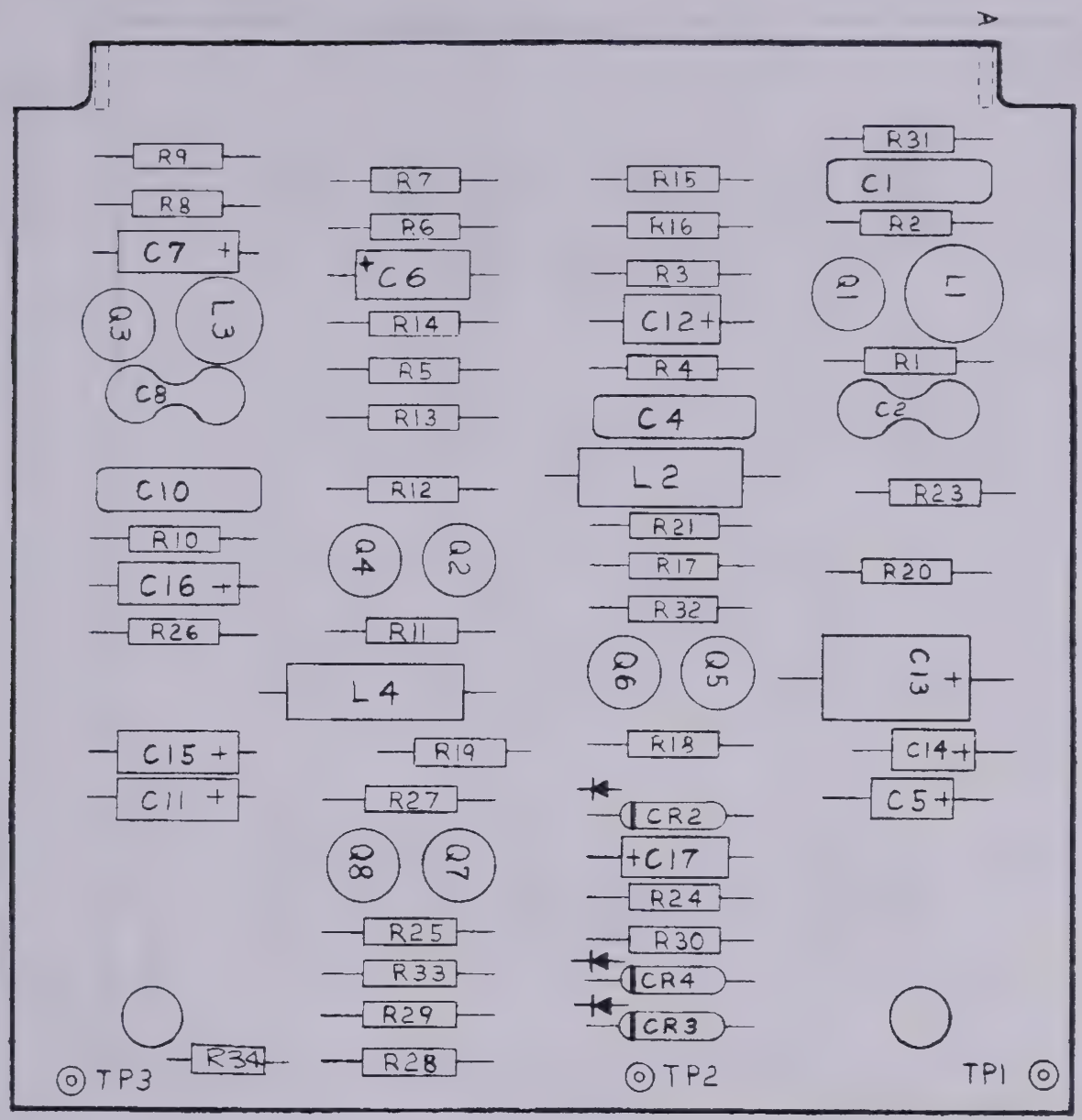


*Figure 5-2. 12.25-kc IF and agc amplifier assembly, A2 (part No. 200139)*

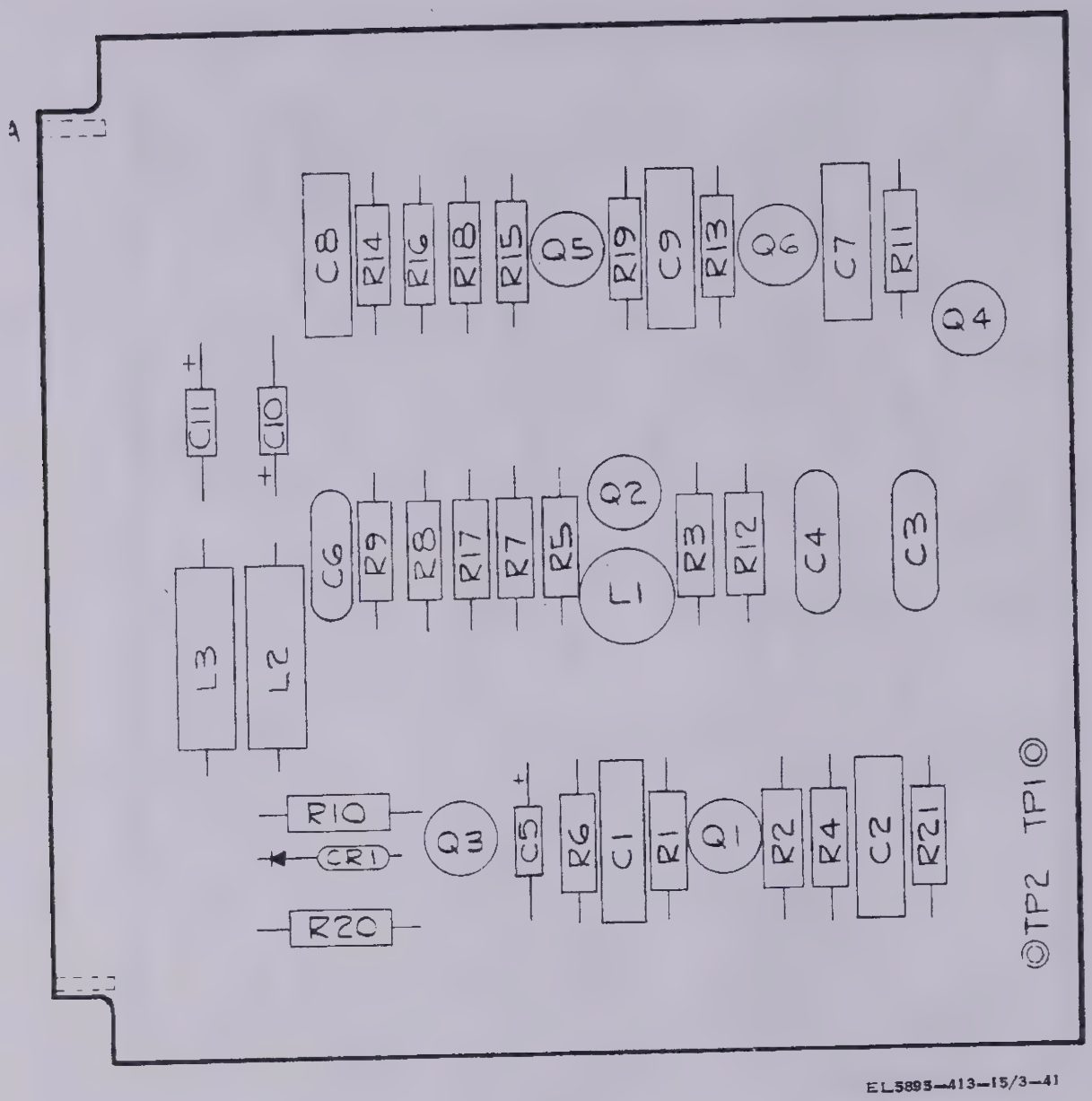


*Figure 5–3. Second mixer assembly, A4 (part No. 200151)*

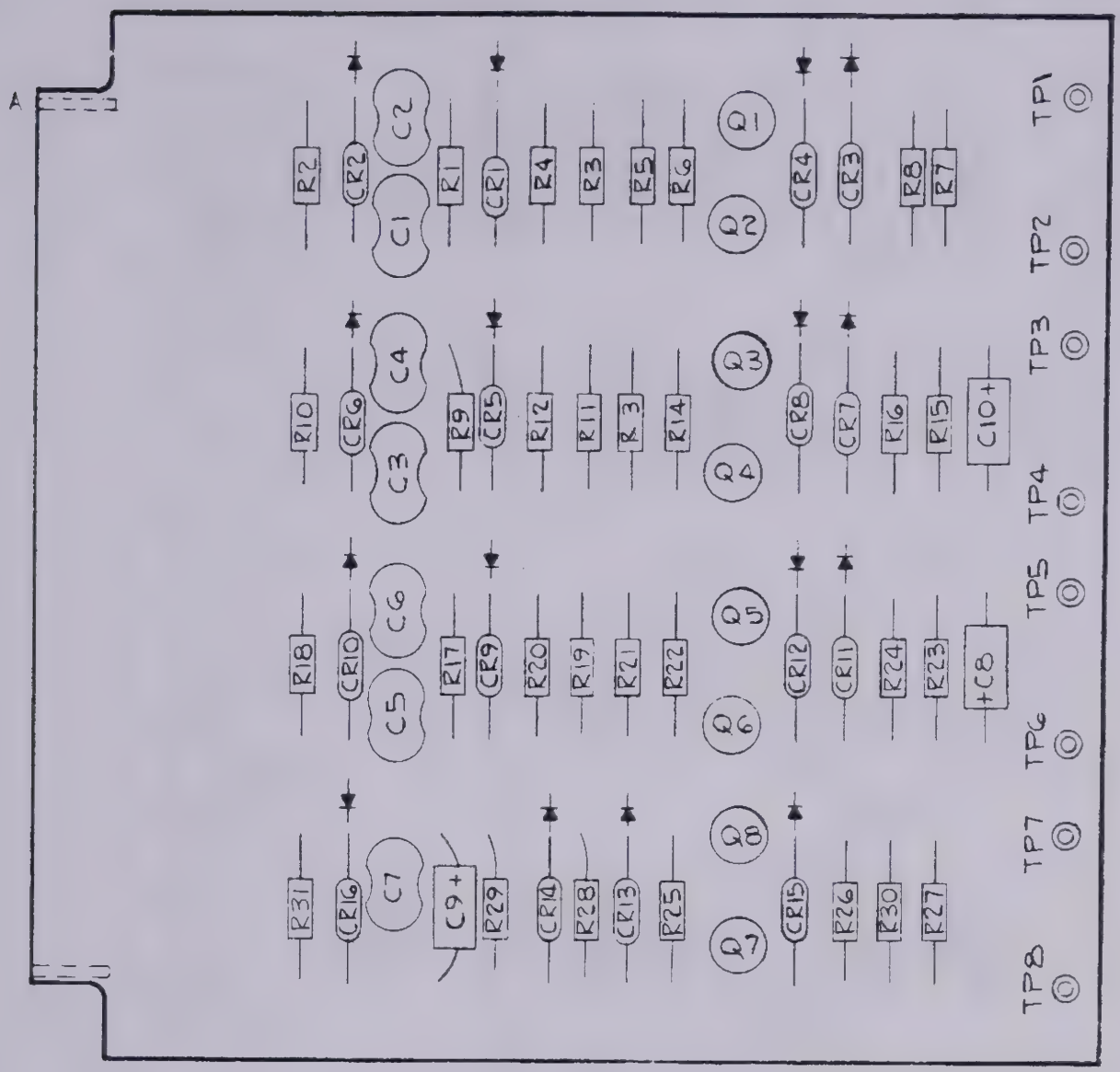


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*Figure 5-4. 45-kc to 11,250-kc three flip-flops and gates assembly, A5 (part No. 200160)*

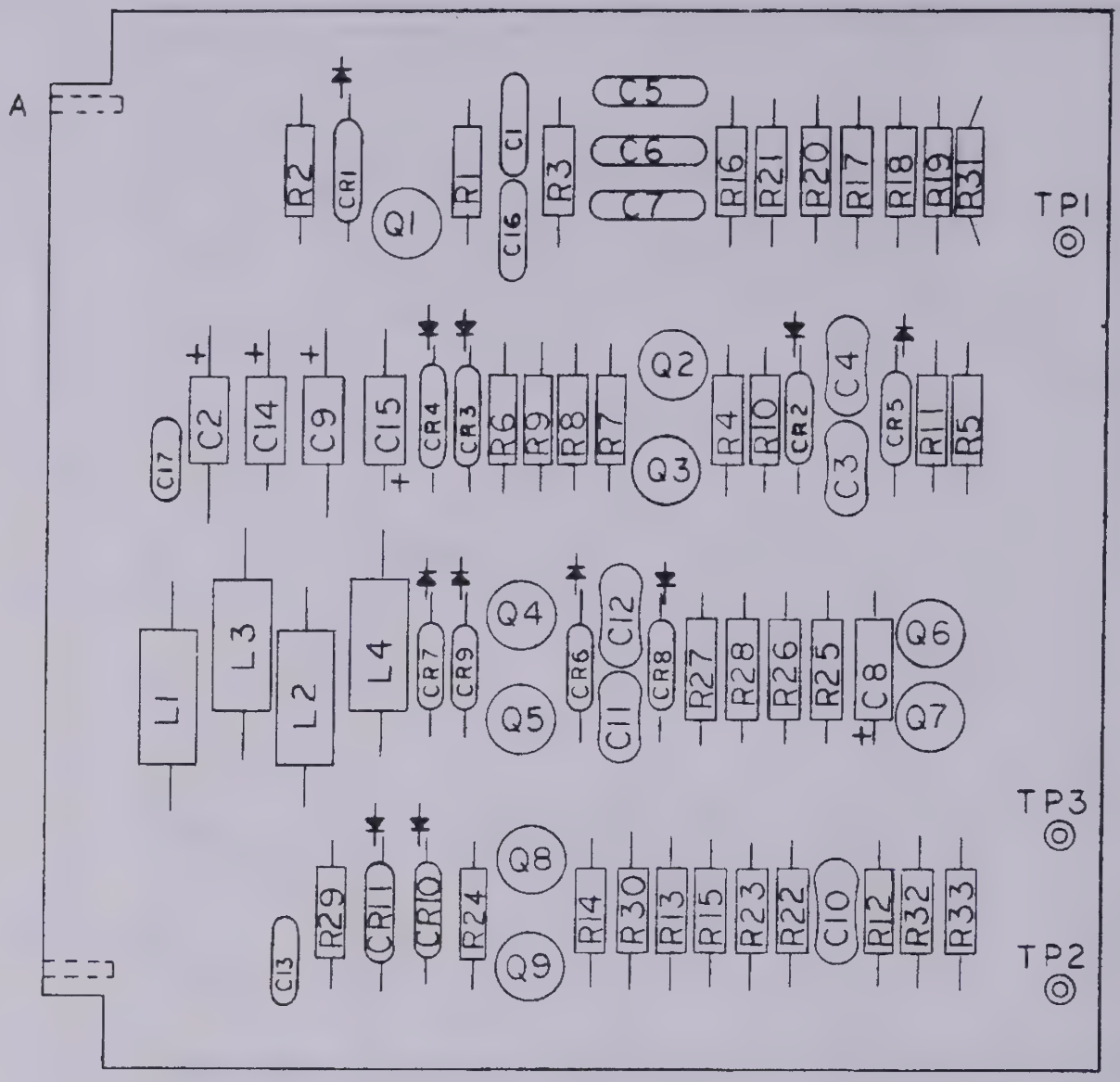


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*Figure 5–5. Local oscillator assembly, A6 (part No. 200163)*

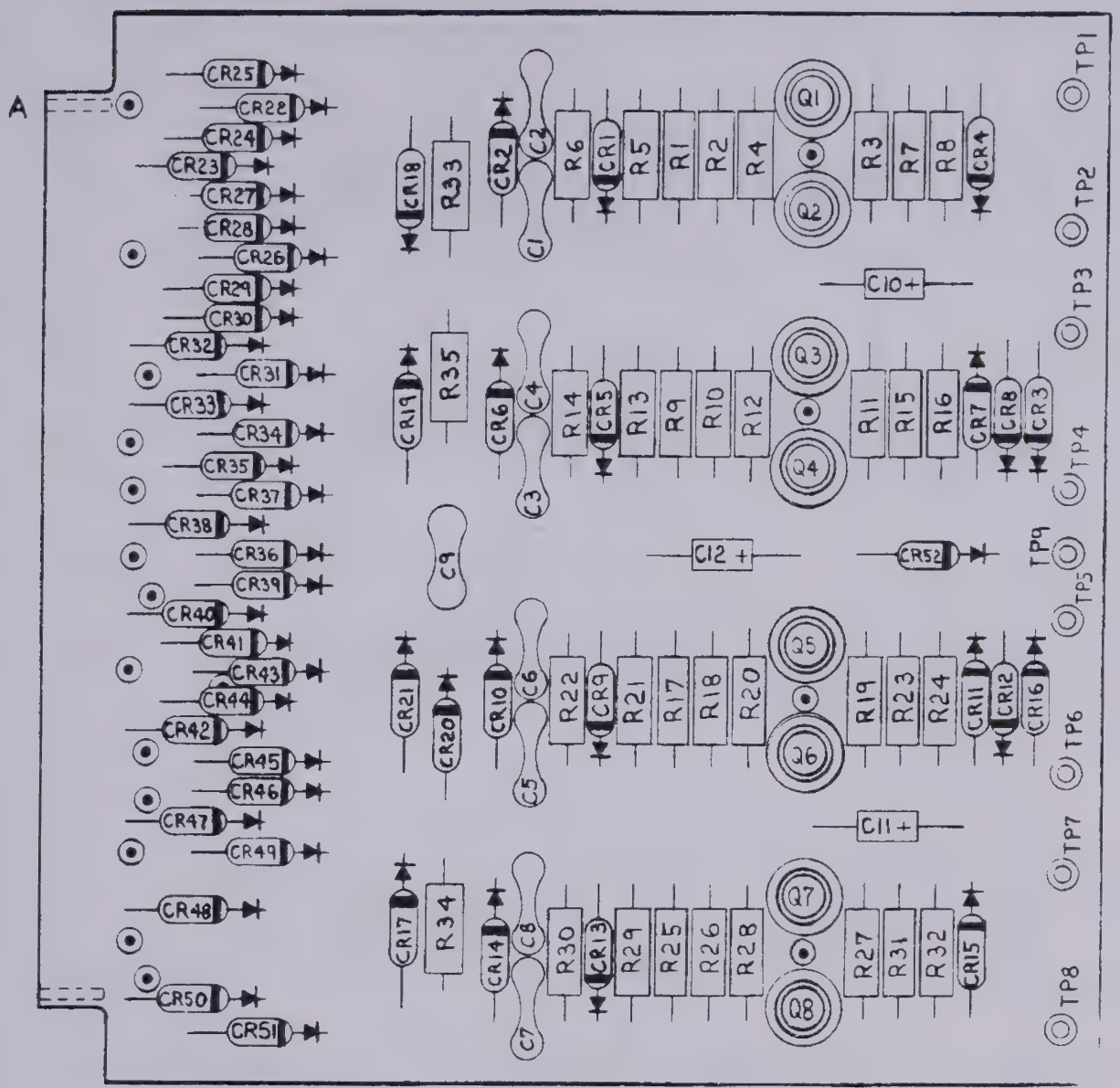


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*Figure 5-6. MOD-10 counter assembly, A7, A8, A21, A22, and A23 (part No. 200022)*

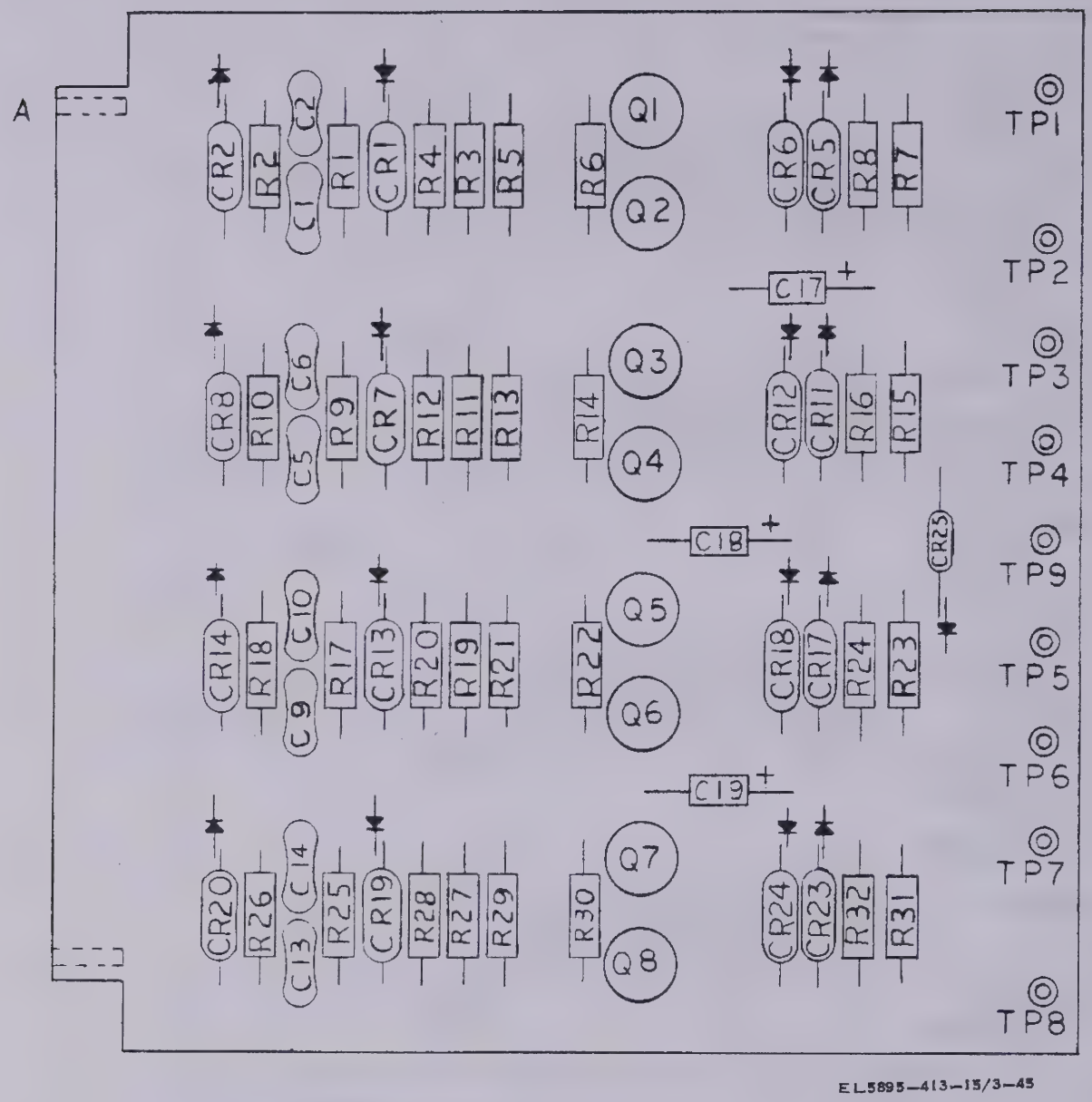


*Figure 5-7. Four flip-flops assembly, A9 (part No. 200016)*

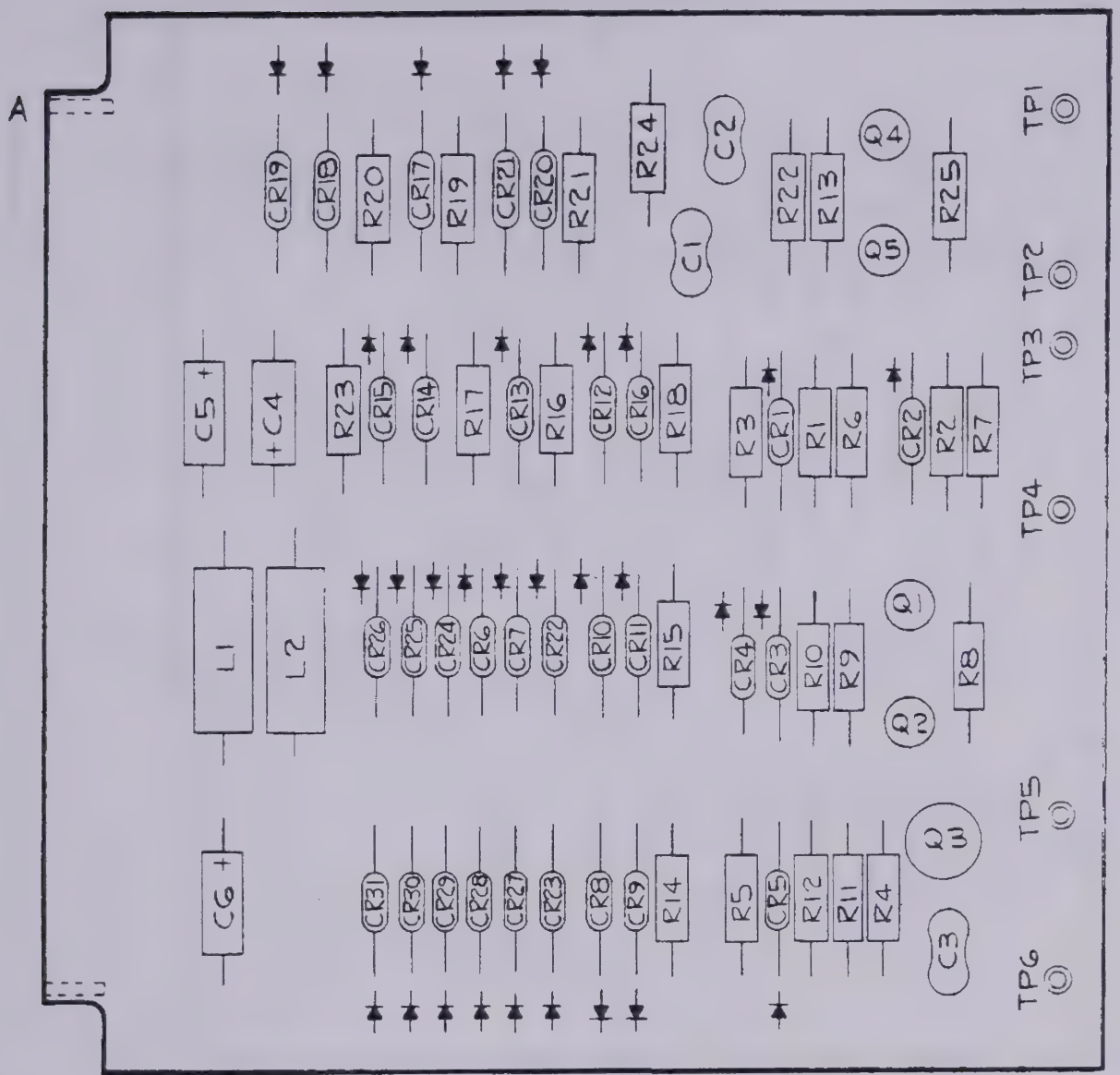


*Figure 5-8. One-shot and reset assembly, A10 (part No. 200157)*

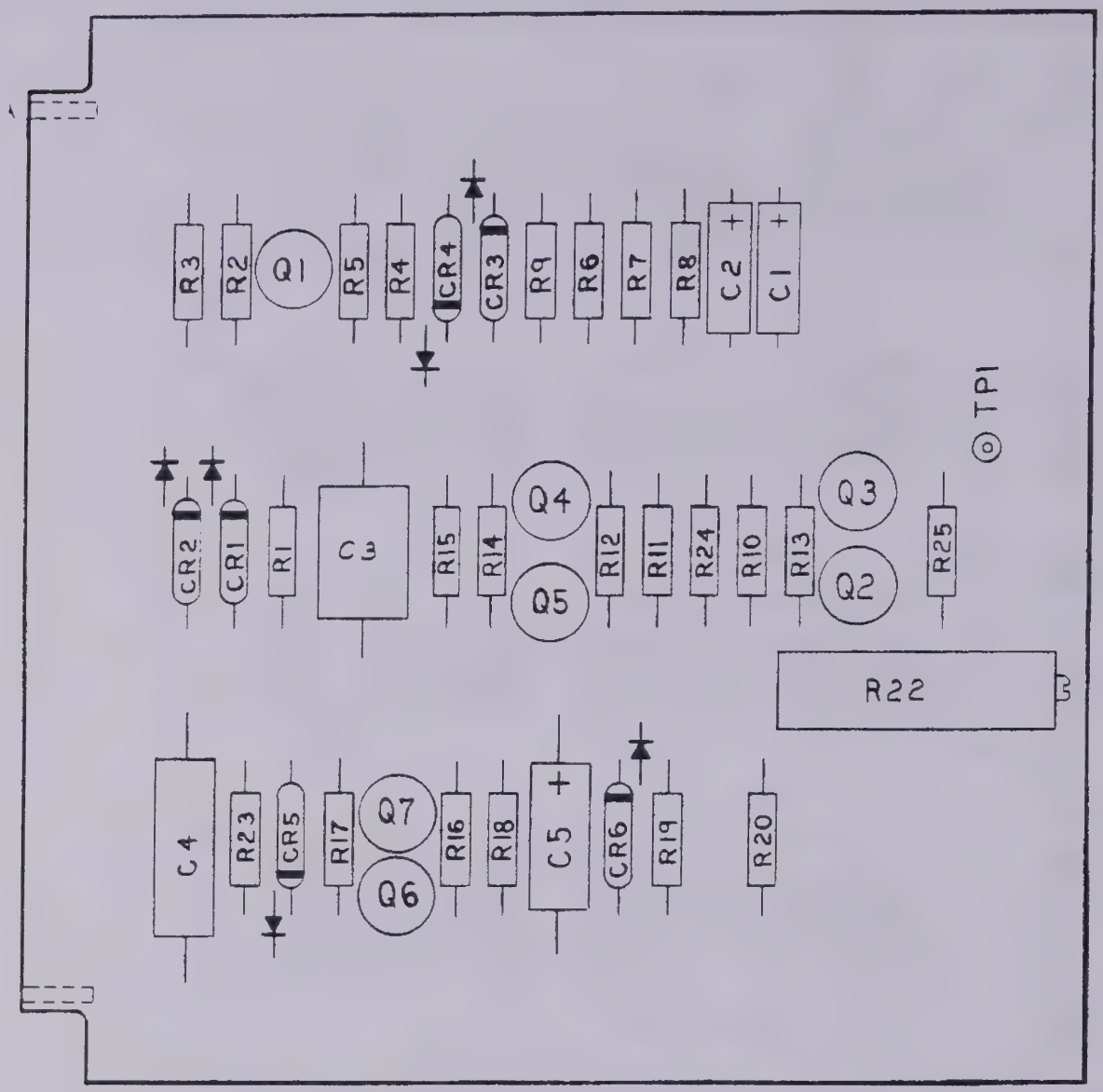


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*Figure 5–9. Synthesizer phase detector (slow-loop) assembly, A12 (part No. 200171)*

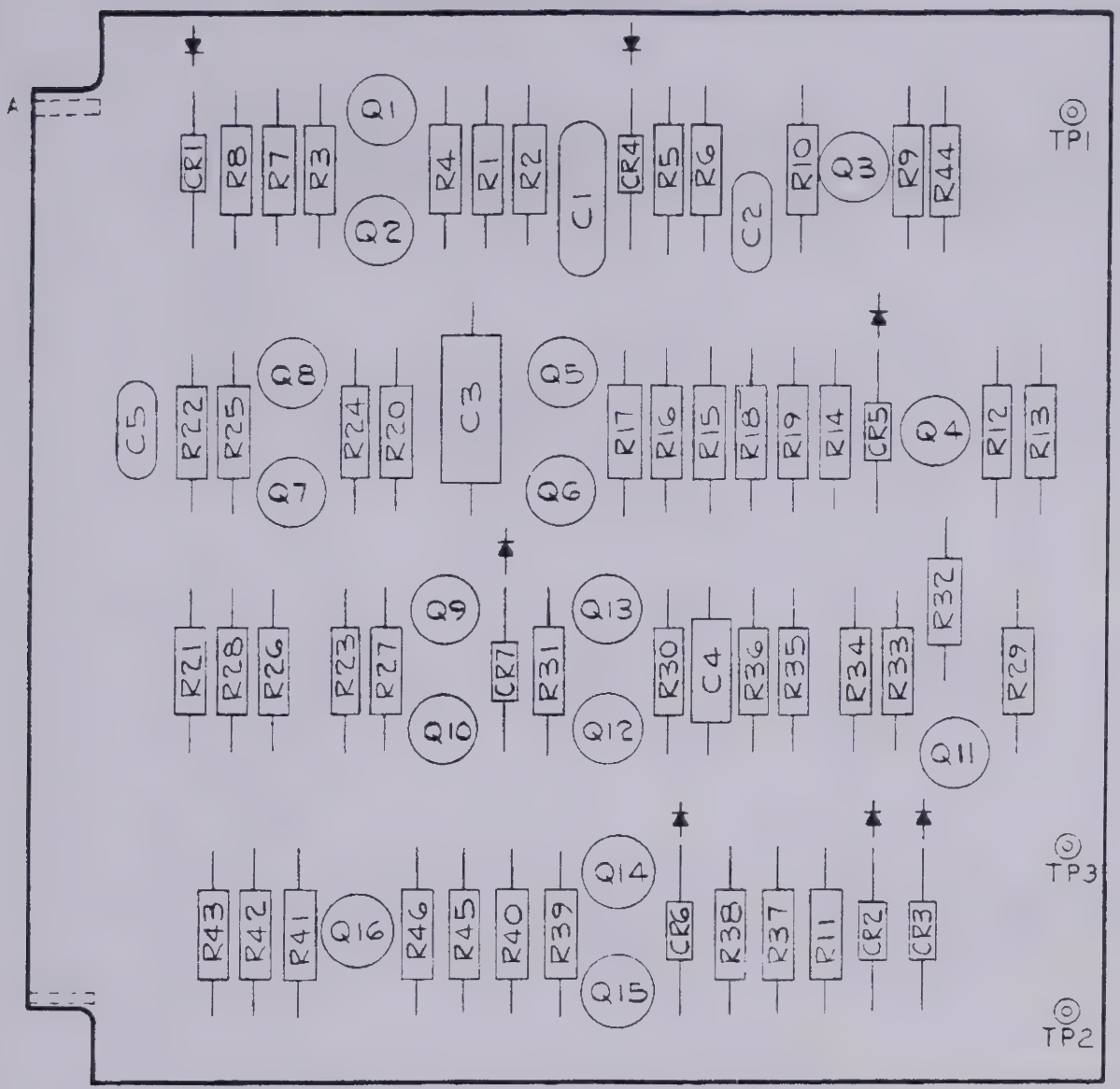


*Figure 5-10. Synthesizer phase detector (fast-loop) assembly, A18 (part No. 200168)*

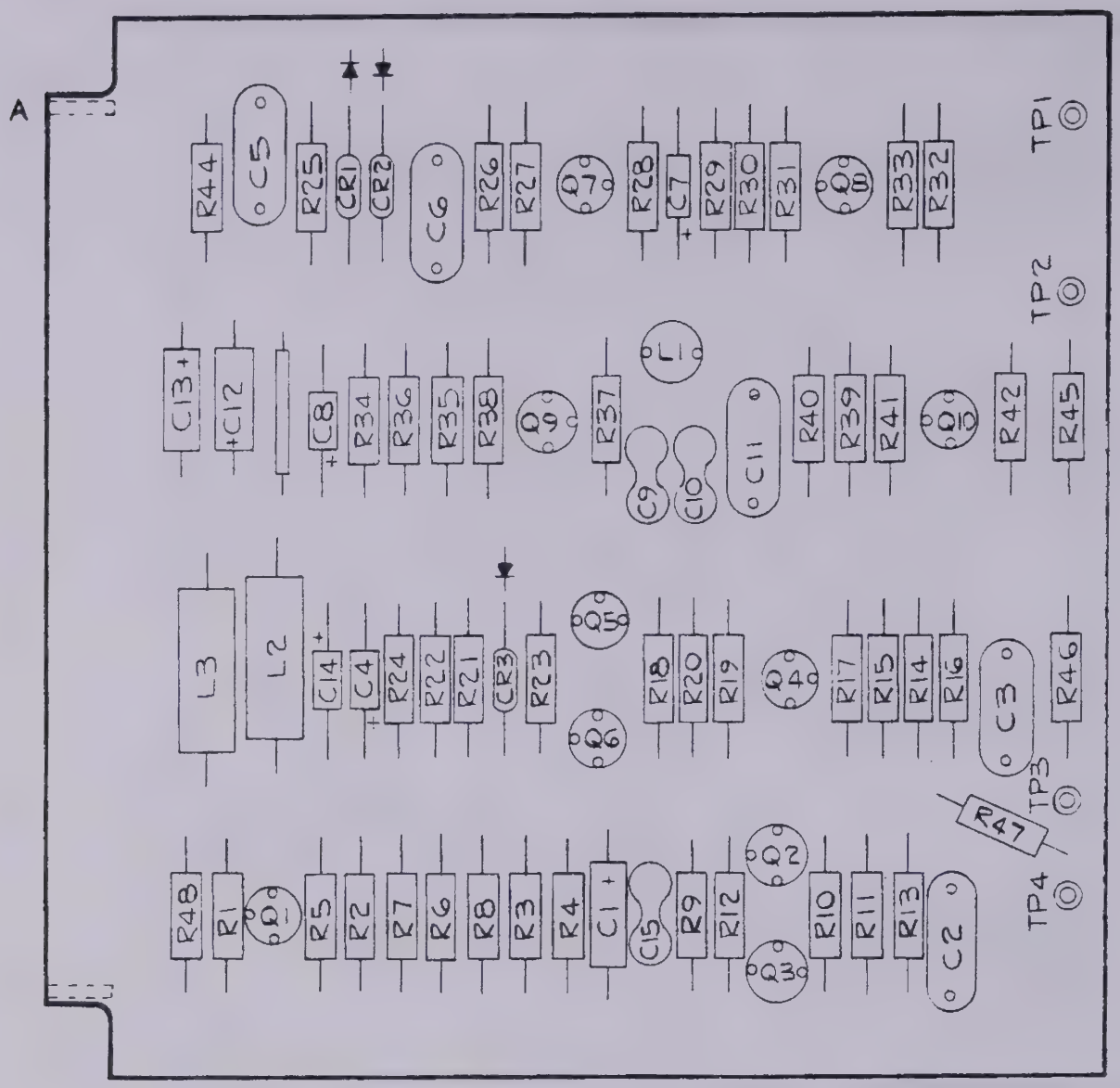


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*Figure 5–11. 100-kc amplifier and phase shifter assembly, A14 (part No. 200154)*

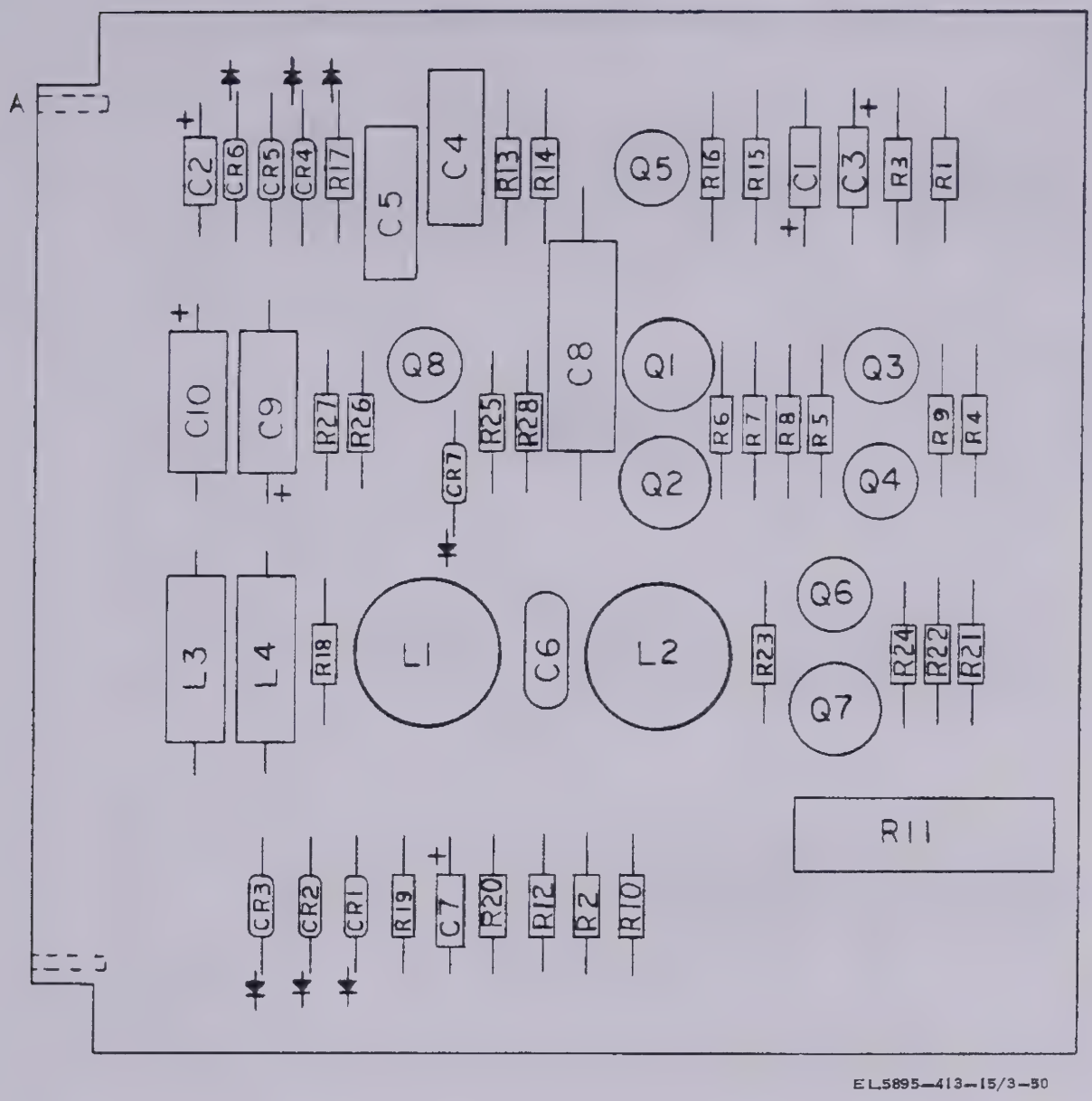


*Figure 5-12. Servo and agc phase detectors assembly, A15 (part No. 200433)*

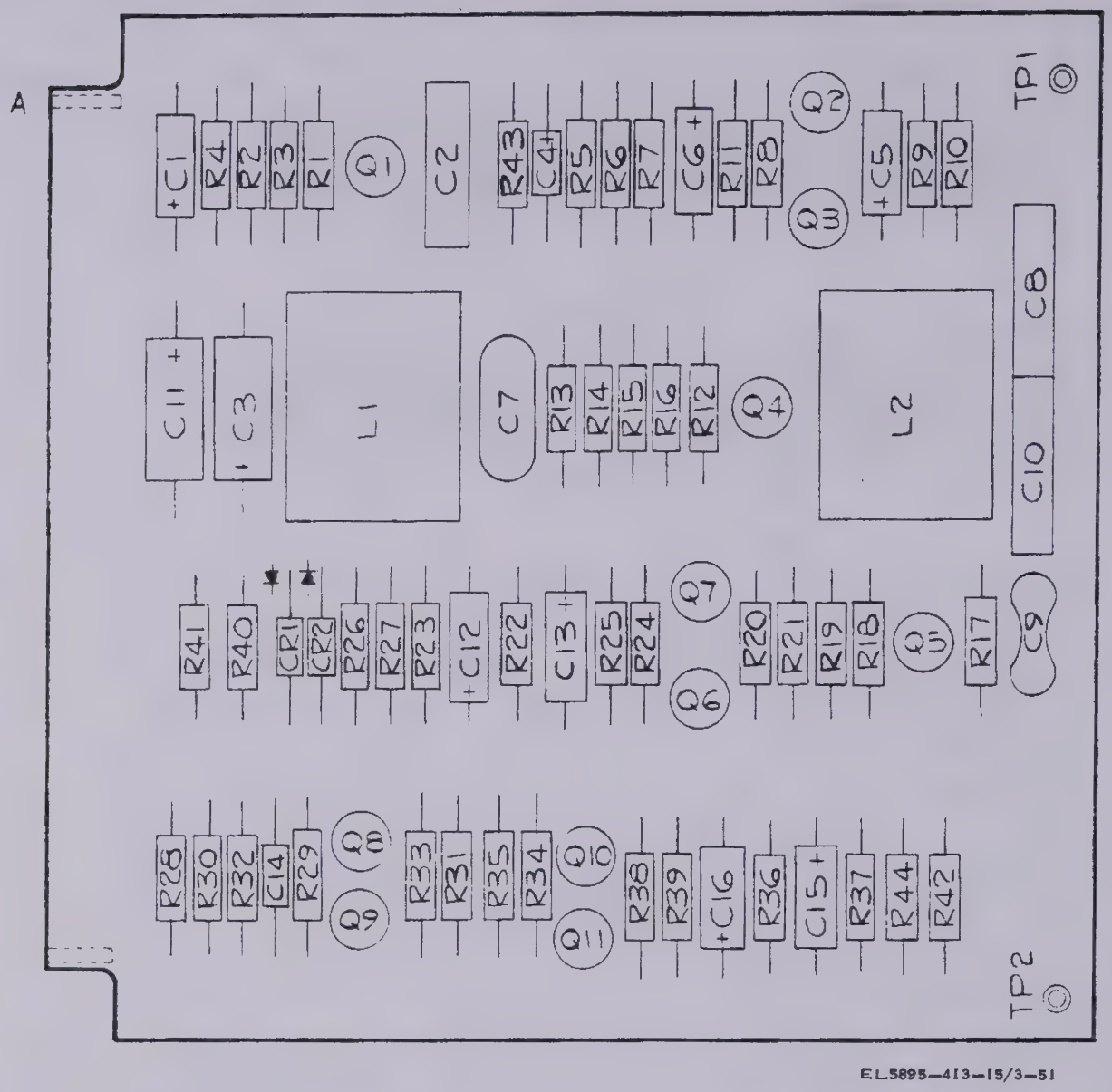


*Figure 5-13. 1-kc IF amplifier assembly, A16 (part No. 200142)*

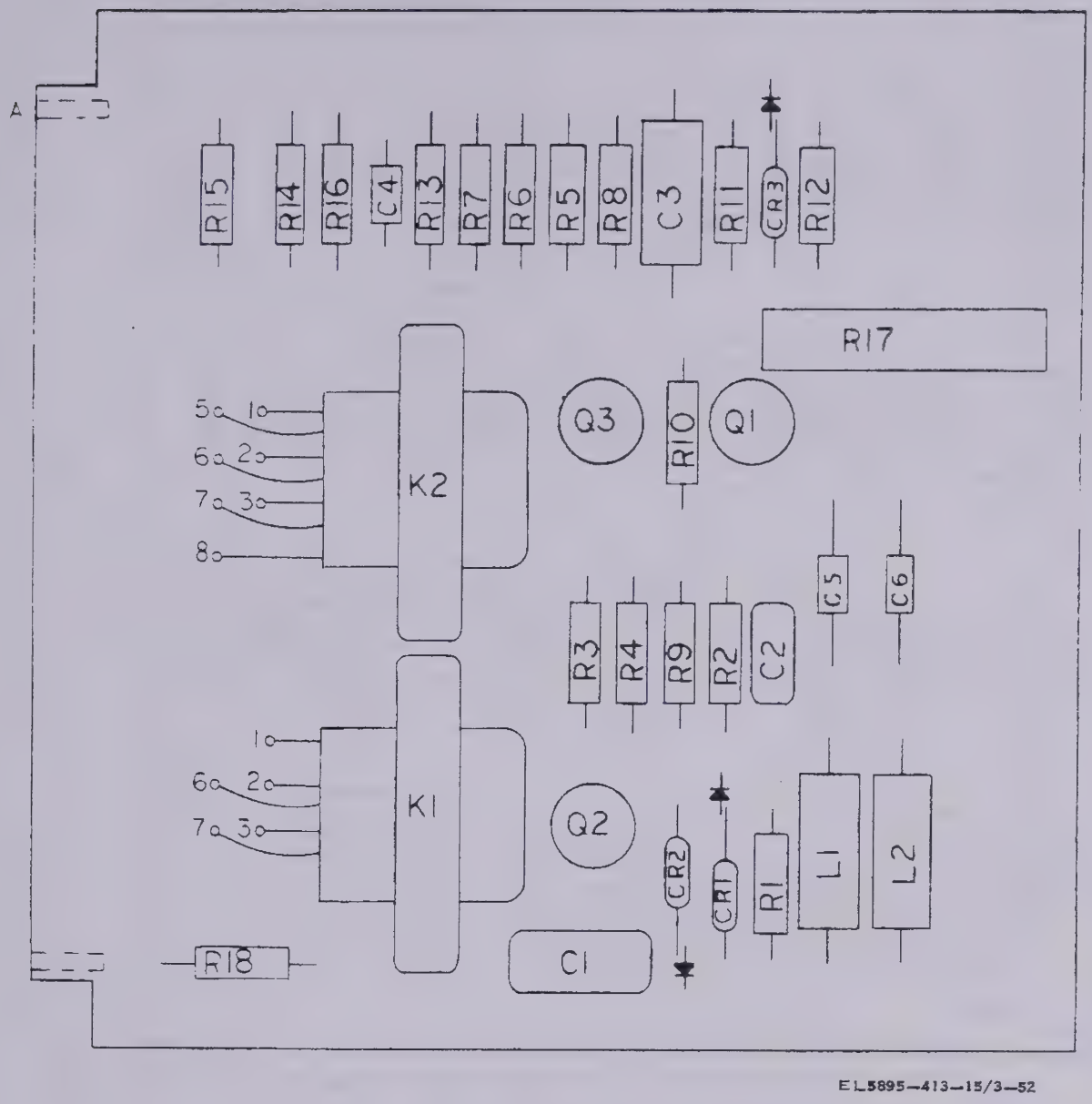


*Figure 5-14. Servo cutout assembly, A17 (part No. 200177)*

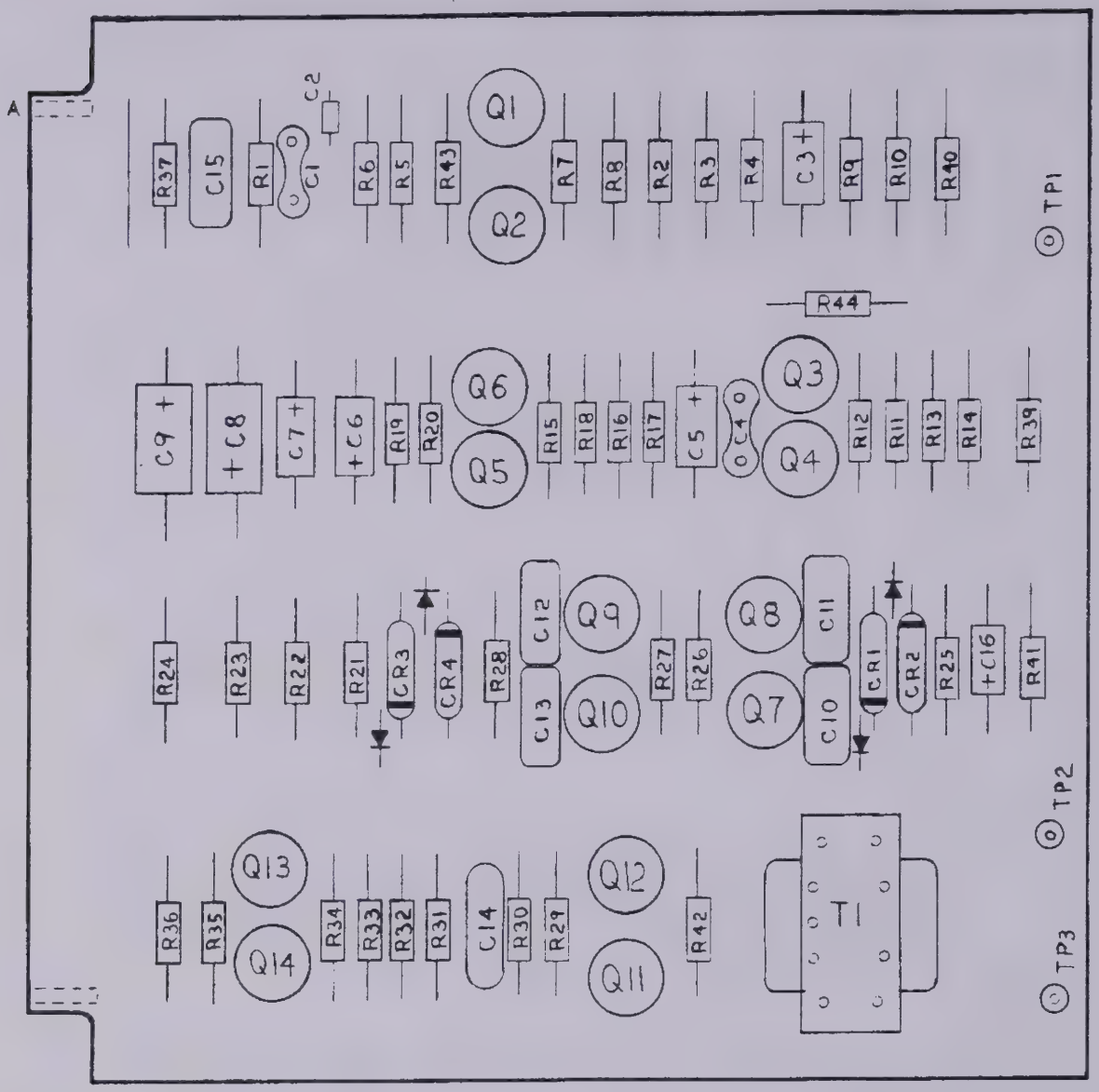


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*Figure 5-15. Servo-motor driver assembly, A18 (part No. 200174)*

*R7 ADDED TO RECEIVERS SERIAL NO. 179, 180

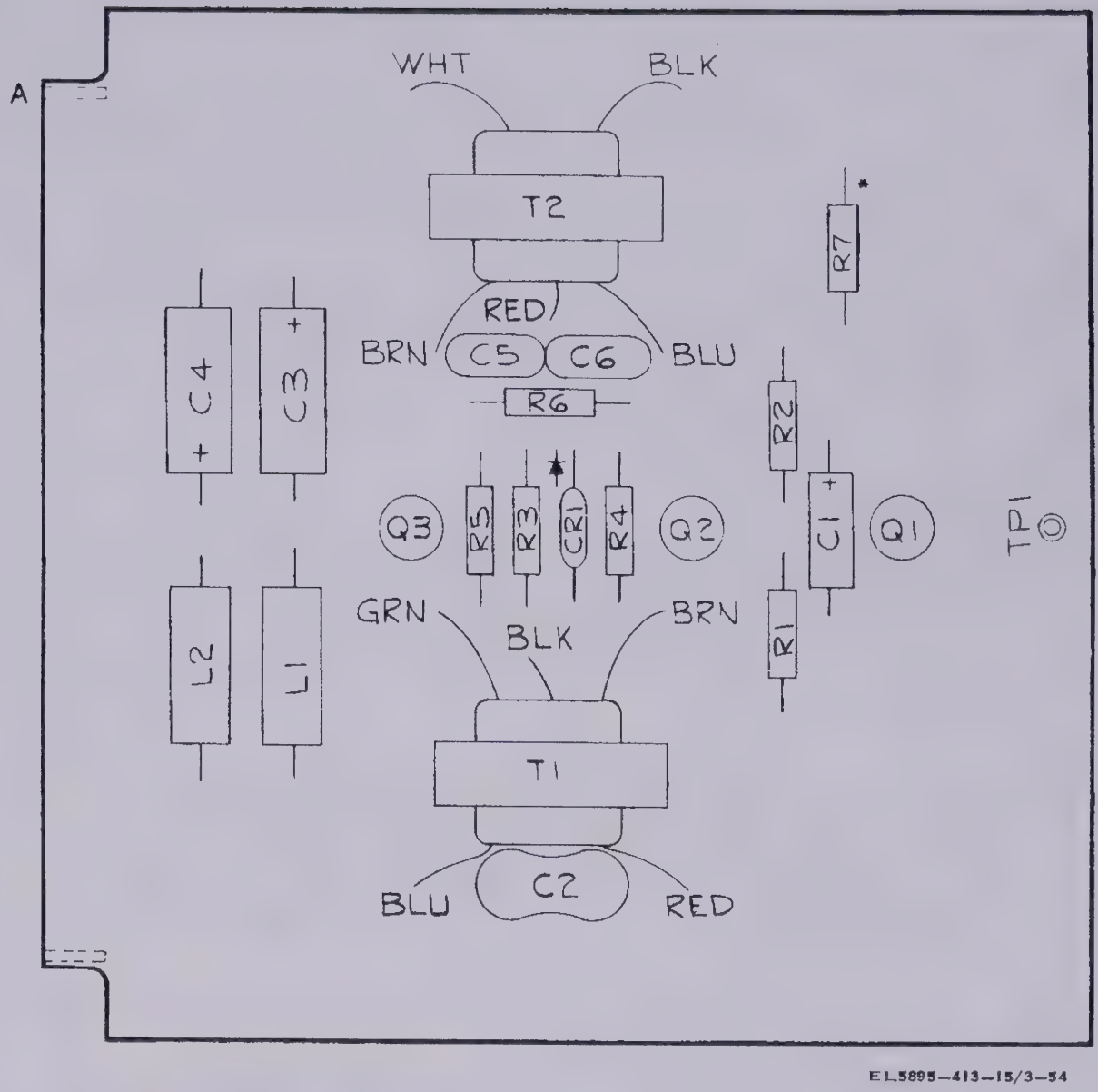
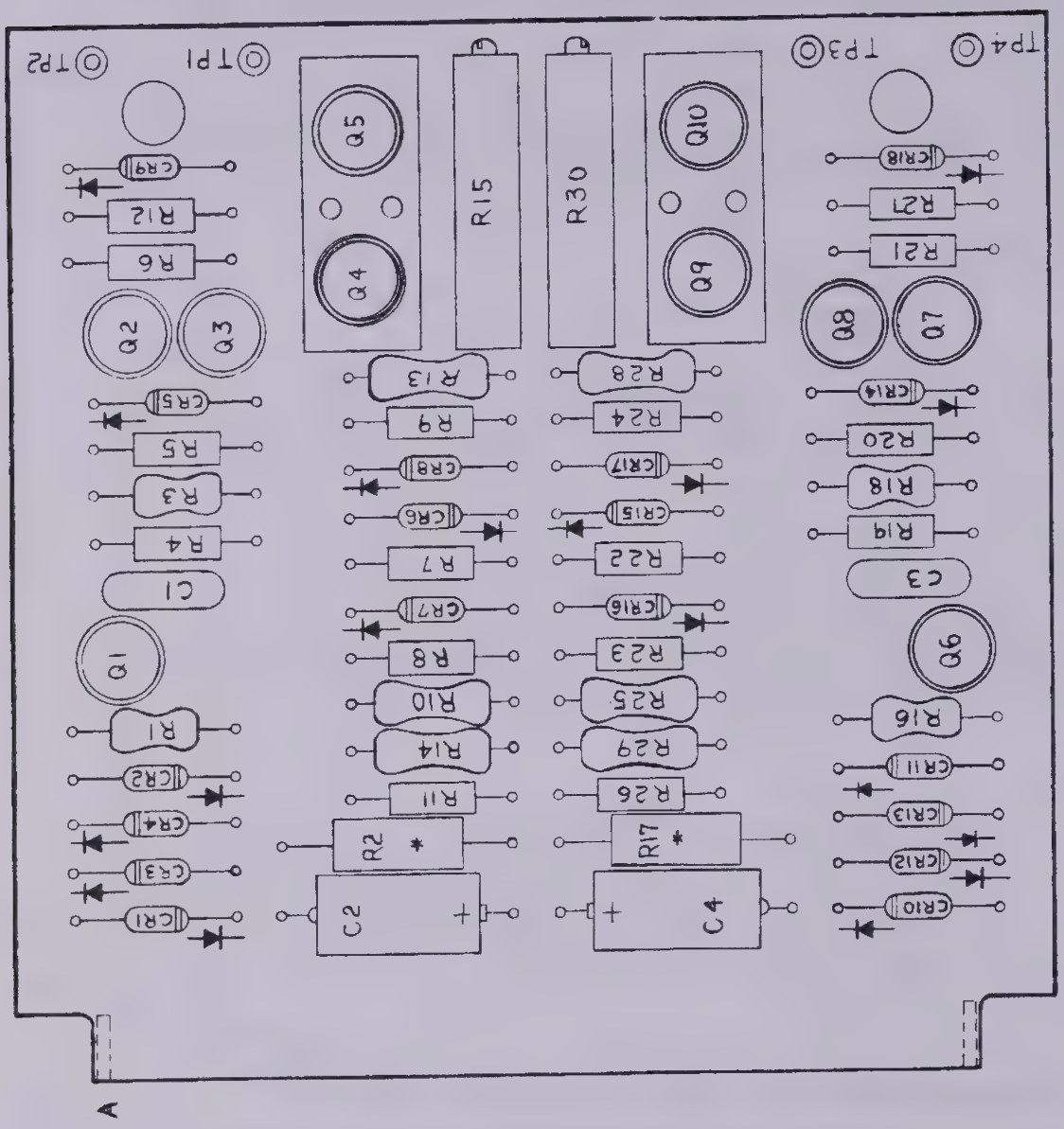



*Figure 5-16. Audio amplifier assembly, A19 (part No. 200136)*

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* R2 & R17, IN RECEIVERS SERIAL NO. 179, 180 REPLACED BY CR19 & CR20 (1N270)

*Figure 5-17. Plus and minus 12-volt power supply assembly, A20 (part No. 200124).*

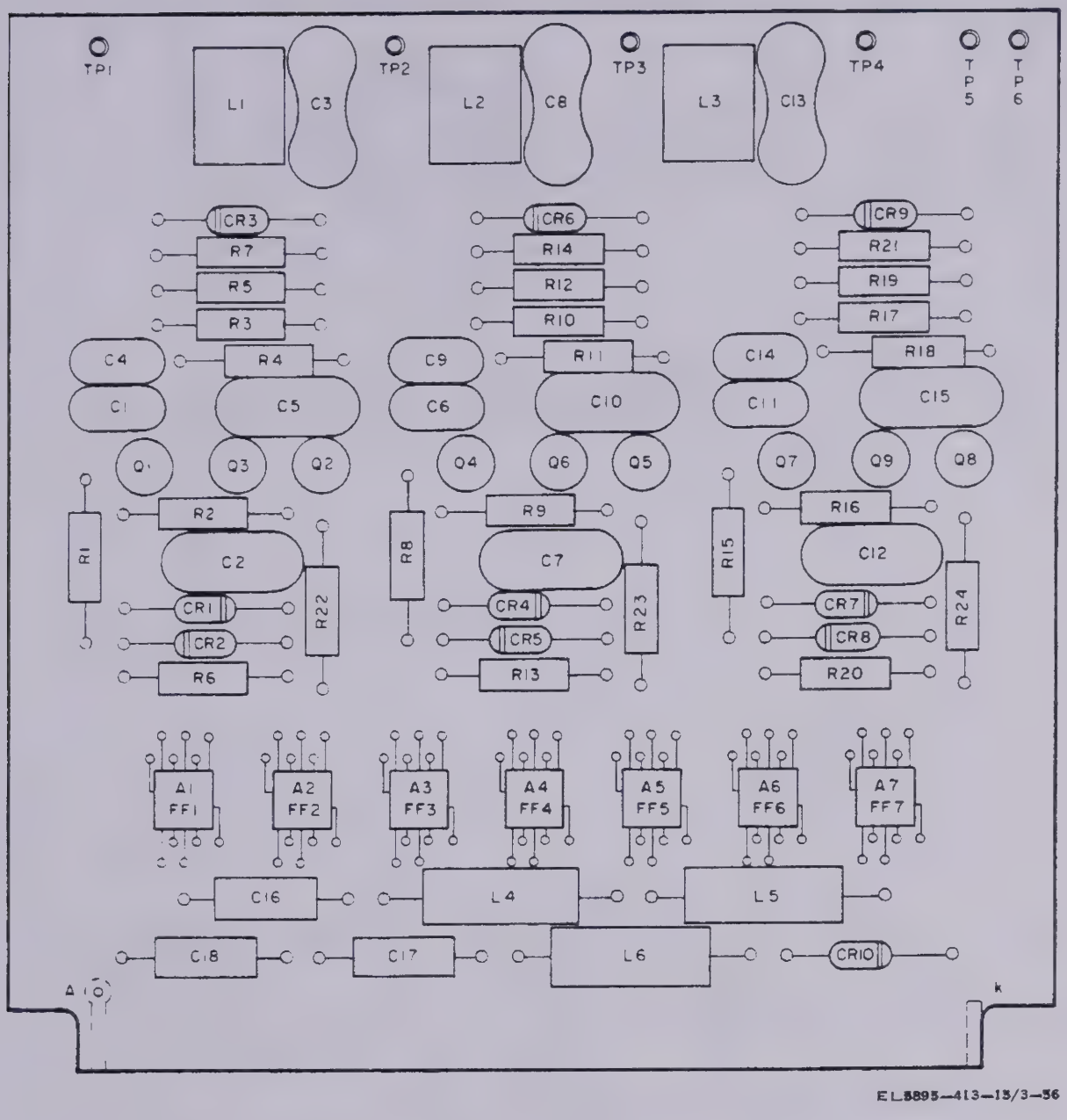



*Figure 5-18. 76.8-kc to 100-kc converter assembly, A24 (part No. 200394)*

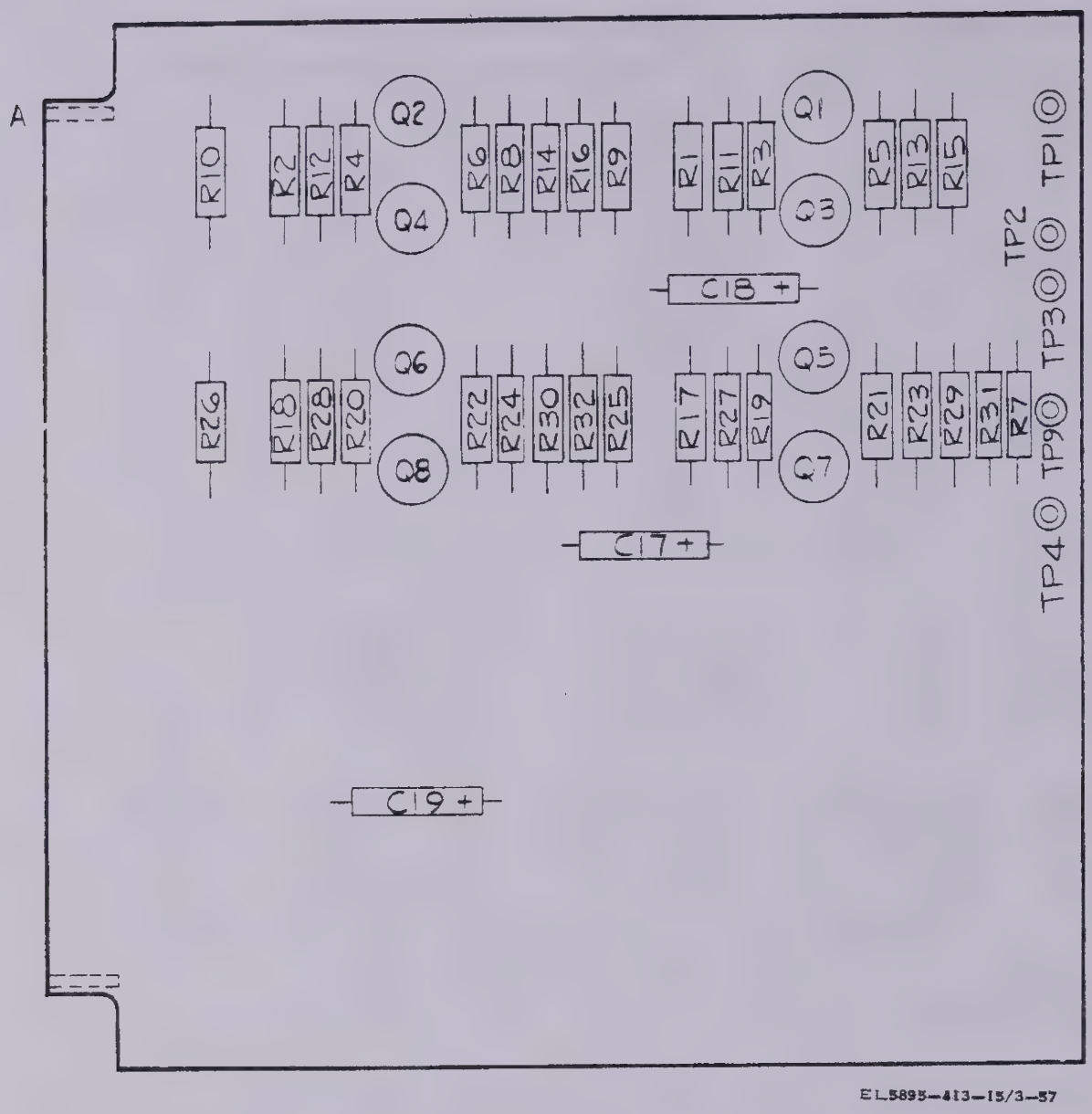



*Figure 5-19. Output buffer assembly, A25 (part No. 200165)*

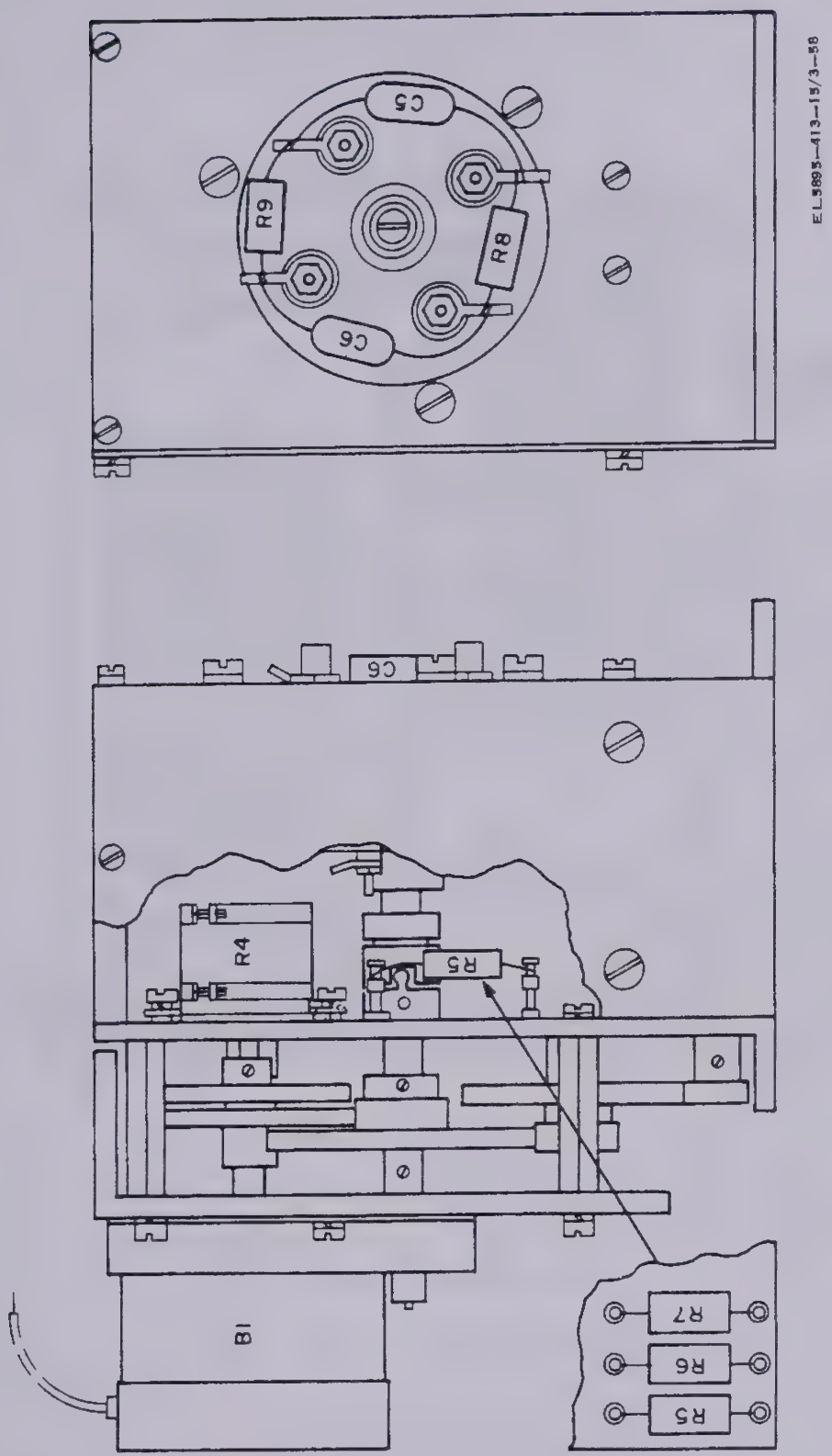



*Figure 5-20. Servo assembly, A27 (part No. 330034)*

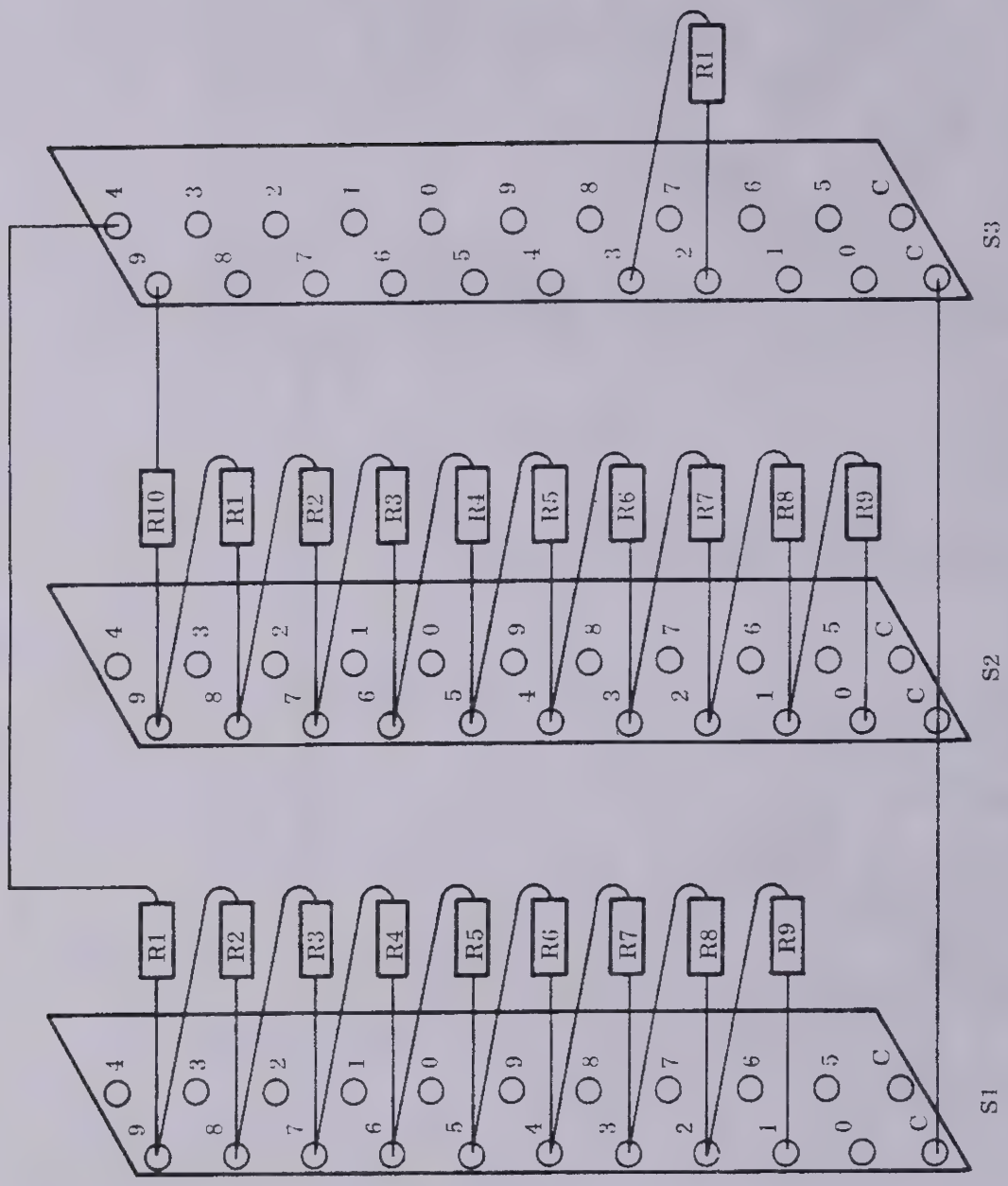
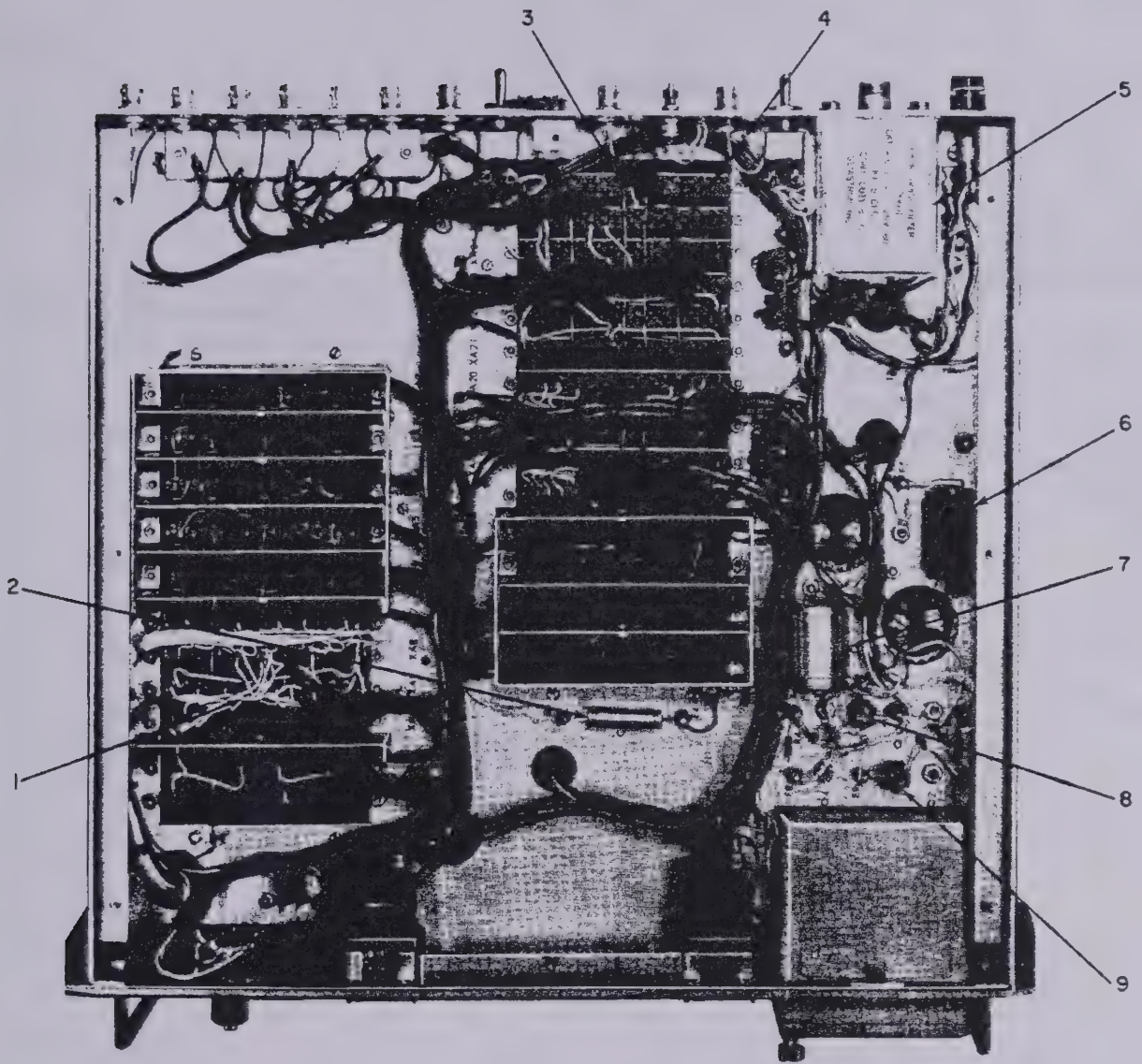



*Figure 5-21. Thumbwheel switch assembly, A28 (part No. 8301011)*




1. CR2 - 6-VOLT CLAMP DIODE
2. C5 - 425 μF, DETECTOR INTEGRATOR
3. CR3 - 10-VOLT CLAMP DIODE
4. CR1 - 6-VOLT CLAMP DIODE
5. FL1 - RFI LINE FILTER
6. C4 - POWER-SUPPLY FILTER
7. C3 - POWER-SUPPLY FILTER
8. Q3 - REGULATOR TRANSISTOR
9. Q1 - REGULATOR TRANSISTOR

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*Figure 5-22. VLF-12B receiver-phase comparator, bottom view*

# APPENDIX

## REFERENCES

| | |
|---|---|
| AFM 66-1 | Maintenance Management (Air Force). |
| Commercial Literature | Test Equipment for Automatic Digital Message Switching Centers AN/FYQ-42(V)1 Through AN/FYQ-42(V)12 and AN/FYQ-42(V)T1. |
| DA Pam 310-4 | Index of Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders. |
| DA Pam 310-7 | U. S. Army Equipment Index of Modification Work Orders. |
| NAVSANDA Publication 2002 | Navy Stock List of Forms and Publications Cognizance Symbol I. |
| NW 00-15PA-1 | Soldering for Electric and Electronic Applications. |
| TB SIG 222 | Solder and Soldering. |
| TB SIG 364 | Field Instructions for Painting and Preserving Electronics Command Equipment. |
| TM 38-750 | Army Equipment Record Procedures. |
| TO-00-25-234 | General Shop Practice Requirements for the Repair, Maintenance and Tests of Electronic Equipment. |
| TO-0-1-01N | Numerical Index and Requirements Tables, Numerical Index, Alphabetical Indexes and Cross Reference Table Technical Orders (ADP Category 00). |
| TO-31-1-75 | Maintenance Engineering Standard General Maintenance Practices. |

By Order of the Secretaries of the Army and the Navy:

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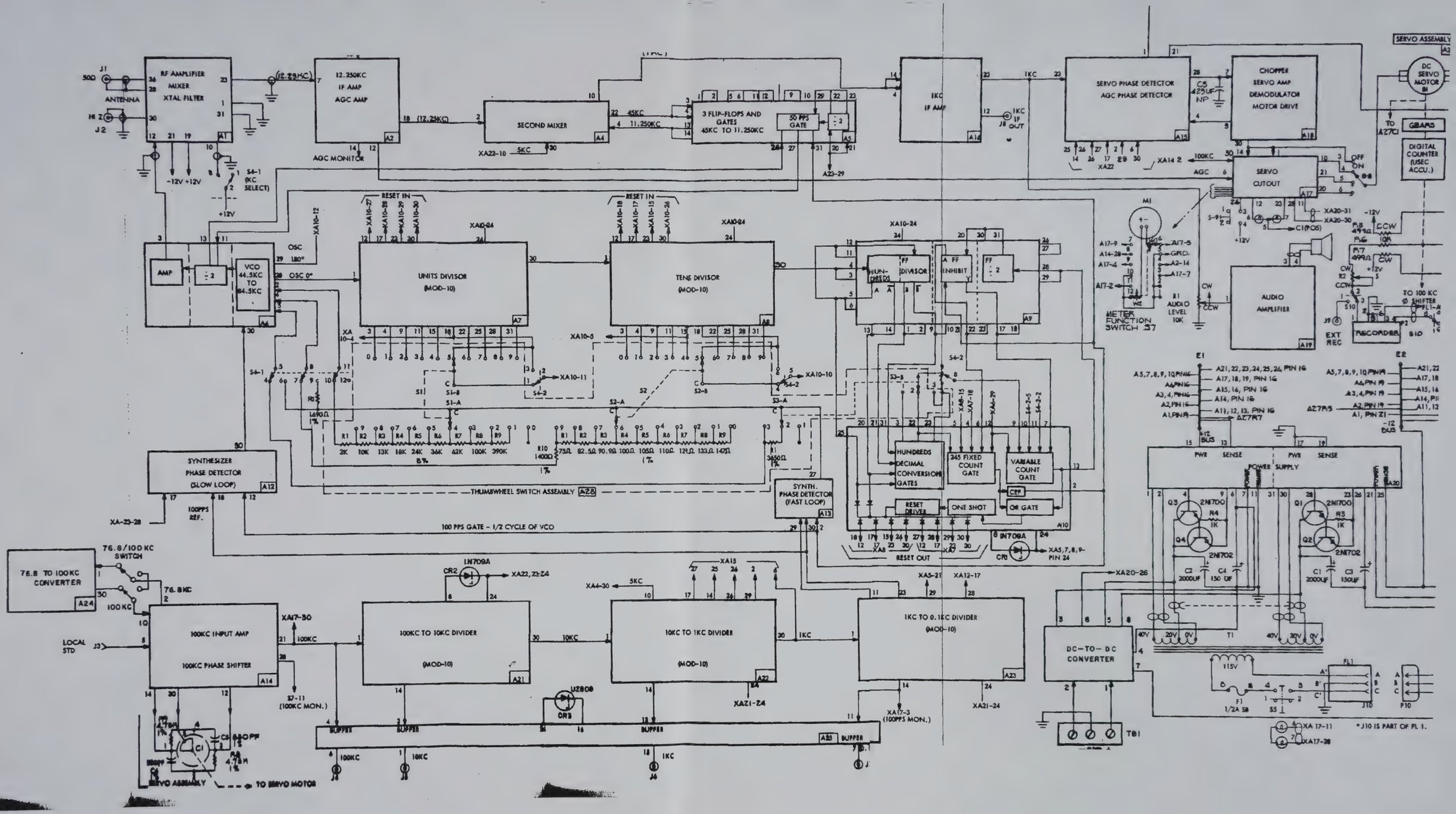
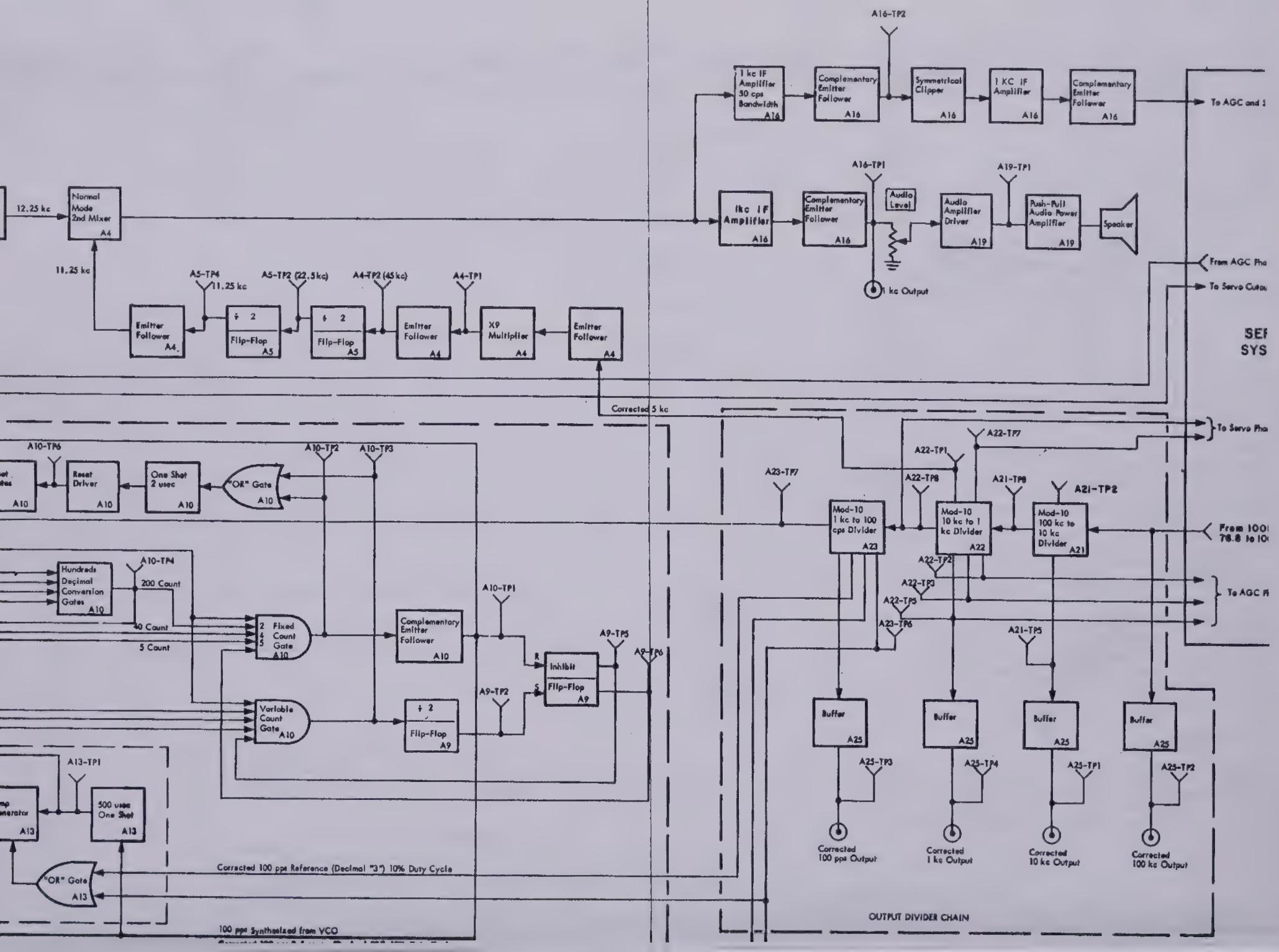
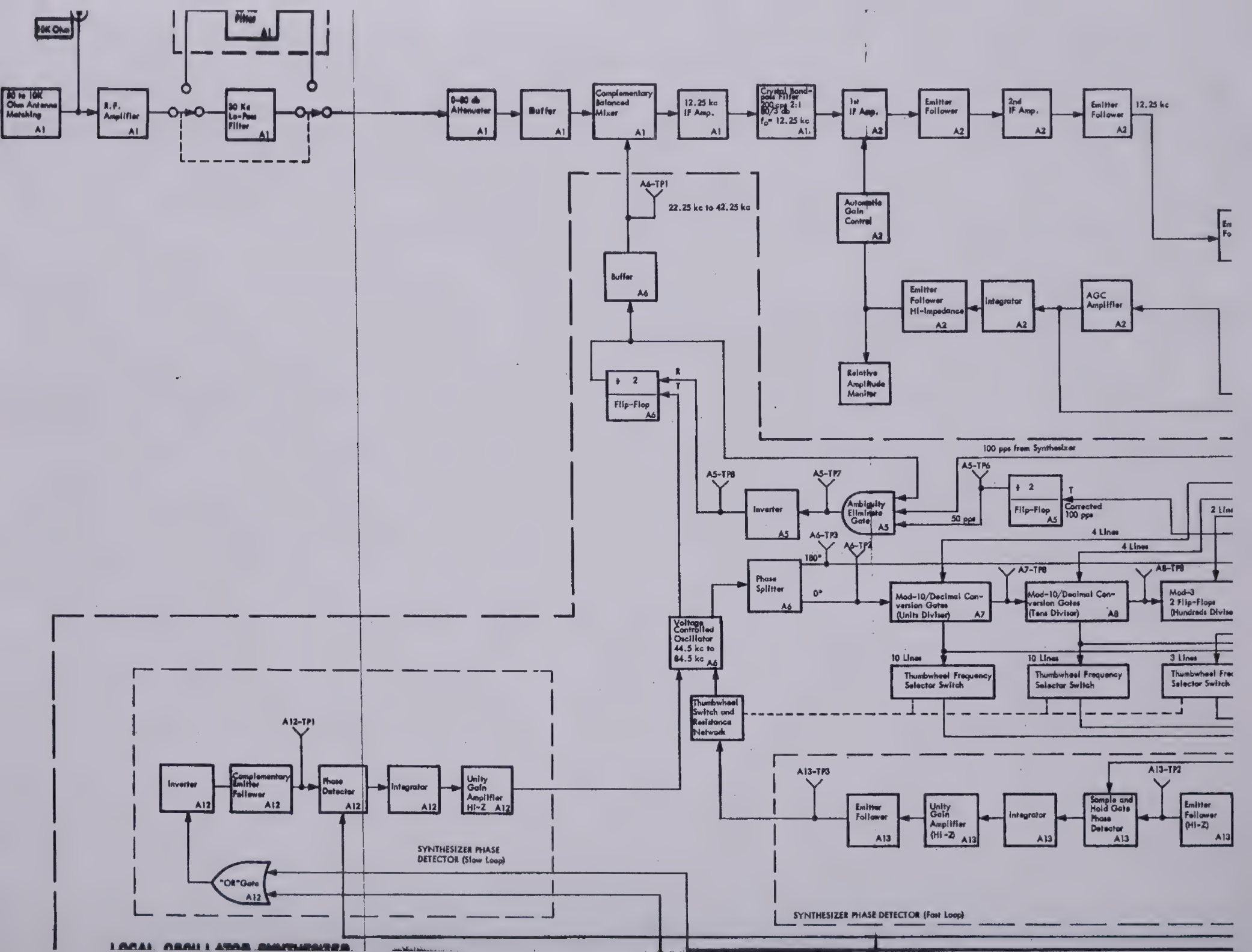
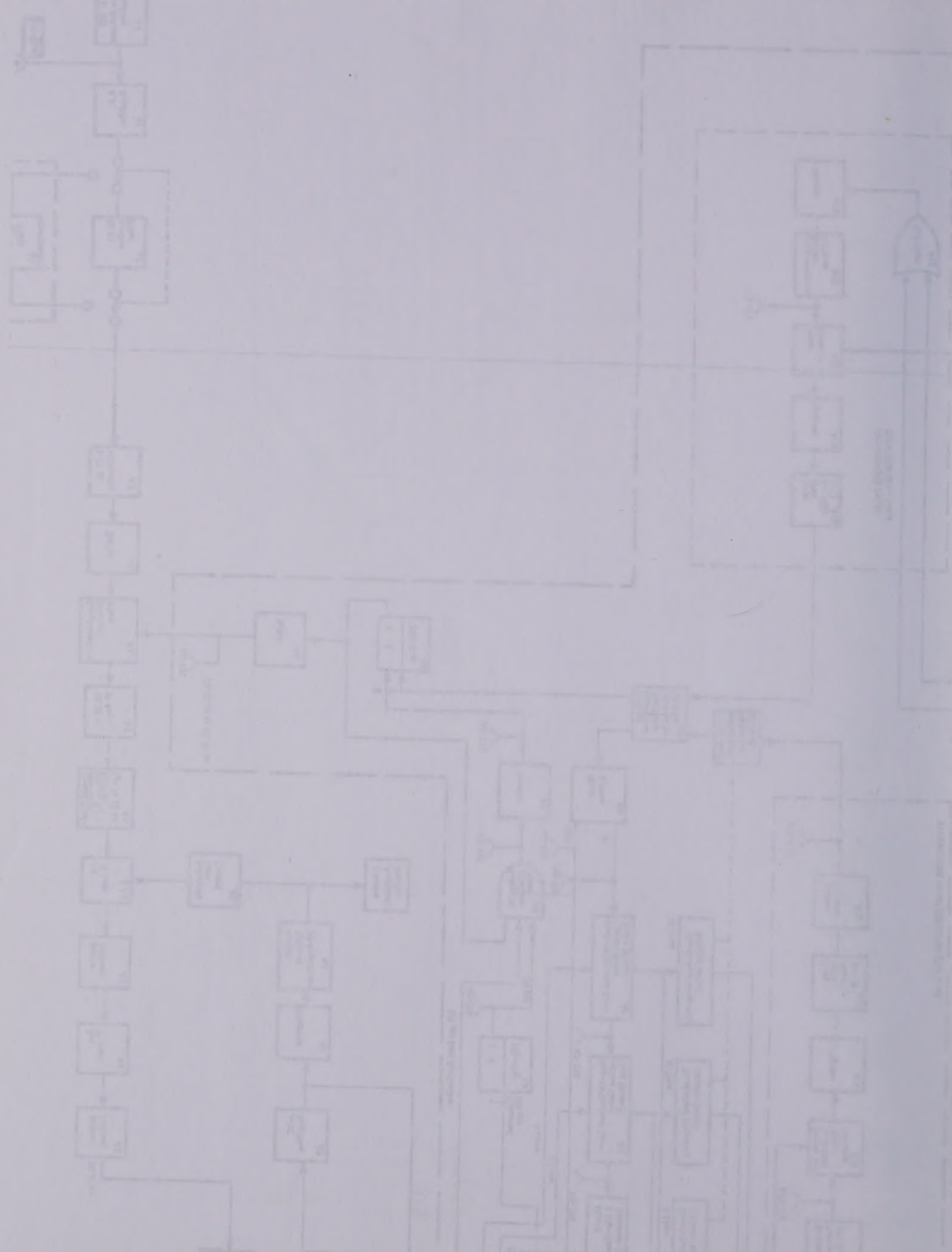
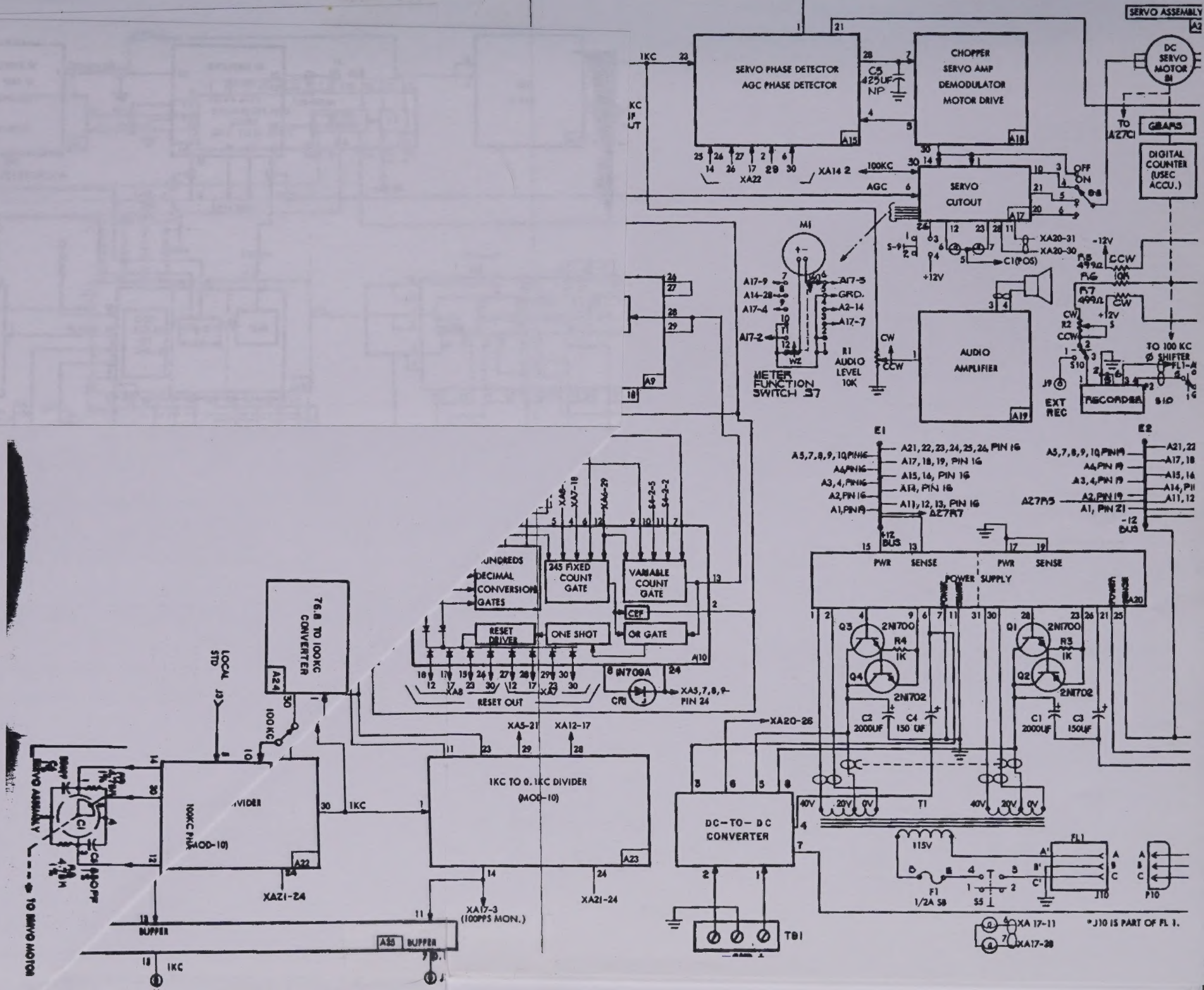
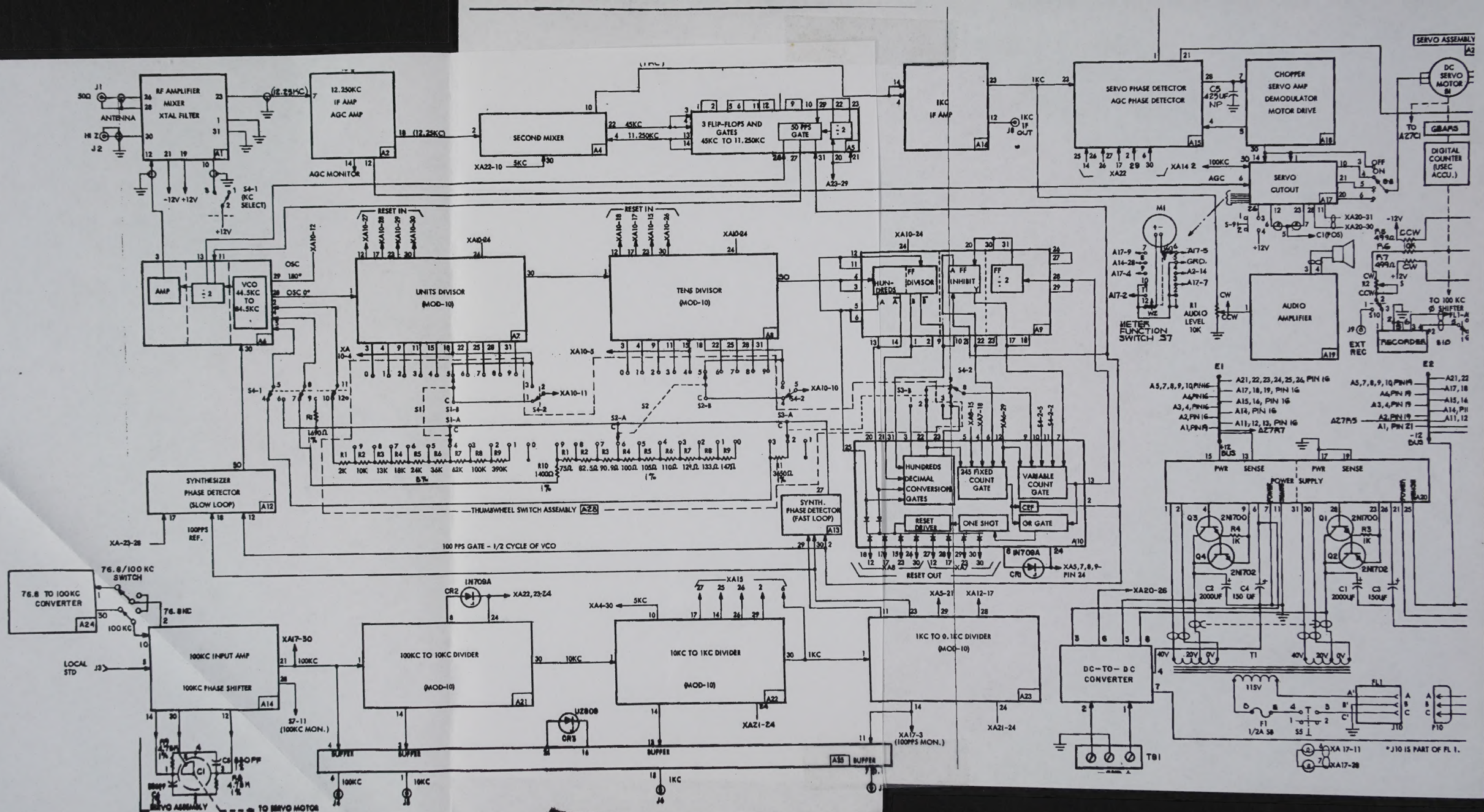

RF AMPLIFIER MIXER XTAL FILTER
12.250KC IF AMP AGC AMP
SECOND MIXER
3 FLIP-FLOPS AND GATES 45KC TO 11.250KC
50 PPS GATE
1KC IF AMP
SERVO PHASE DETECTOR AGC PHASE DETECTOR
CHOPPER SERVO AMP DEMODULATOR MOTOR DRIVE
SERVO ASSEMBLY
DC SERVO MOTOR
GEARS
DIGITAL COUNTER (USEC ACCU.)
SERVO CUTOUT
ANTENNA
AGC MONITOR
S4-1 (KC SELECT)
AMP
VCO 44.5KC TO 84.5KC
OSC
UNITS DIVISOR (MOD-10)
TENS DIVISOR (MOD-10)
HUN-DREDS DIVISOR
A FF INHIBIT
METER FUNCTION SWITCH S7
R1 AUDIO LEVEL 10K
AUDIO AMPLIFIER
EXT REC
RECORDER
SYNTHESIZER PHASE DETECTOR (SLOW LOOP)
THUMBWHEEL SWITCH ASSEMBLY A28
SYNTH. PHASE DETECTOR (FAST LOOP)
100 PPS GATE – 1/2 CYCLE OF VCO
HUNDREDS DECIMAL CONVERSION GATES
245 FIXED COUNT GATE
VARIABLE COUNT GATE
RESET DRIVER
ONE SHOT
OR GATE
RESET OUT
POWER SUPPLY
76.8 TO 100KC CONVERTER
76.8/100 KC SWITCH
100KC INPUT AMP
100KC PHASE SHIFTER
100KC TO 10KC DIVIDER (MOD-10)
10KC TO 1KC DIVIDER (MOD-10)
1KC TO 0.1KC DIVIDER (MOD-10)
BUFFER
SERVO ASSEMBLY
TO SERVO MOTOR
DC–TO–DC CONVERTER
TB1
*J10 IS PART OF FL 1.


A16-TP2
1 kc IF Amplifier 30 cps Bandwidth A16
Complementary Emitter Follower A16
Symmetrical Clipper A16
1 KC IF Amplifier A16
Complementary Emitter Follower A16
To AGC and
A16-TP1
A19-TP1
1kc IF Amplifier A16
Complementary Emitter Follower A16
Audio Level
Audio Amplifier Driver A19
Push-Pull Audio Power Amplifier A19
Speaker
1 kc Output
12.25 kc
Normal Mode 2nd Mixer A4
11.25 kc
A5-TP4 11.25 kc
A5-TP2 (22.5 kc)
A4-TP2 (45 kc)
A4-TP1
Emitter Follower A4
÷ 2 Flip-Flop A5
÷ 2 Flip-Flop A5
Emitter Follower A4
X9 Multiplier A4
Emitter Follower A4
From AGC Pha
To Servo Outpu
SE
SYS
Corrected 5 kc
To Servo Pha
A10-TP6
A10-TP2
A10-TP3
Reset Driver A10
One Shot 2 usec A10
"OR" Gate A10
A22-TP7
A22-TP1
A23-TP7
A22-TP8
A21-TP8
A21-TP2
Mod-10 1 kc to 100 cps Divider A23
Mod-10 10 kc to 1 kc Divider A22
Mod-10 100 kc to 10 kc Divider A21
From 100
78.8 to 10
A22-TP2
A22-TP3
A22-TP5
A23-TP6
To AGC Fi
A21-TP5
Hundreds Decimal Conversion Gates A10
A10-TP4
200 Count
40 Count
5 Count
2 Fixed 4 Count 5 Gate A10
Complementary Emitter Follower A10
A10-TP1
A9-TP5
A9-TP6
Inhibit Flip-Flop A9
A9-TP2
Variable Count Gate A10
÷ 2 Flip-Flop A9
Buffer A25
Buffer A25
Buffer A25
Buffer A25
A25-TP3
A25-TP4
A25-TP1
A25-TP2
Corrected 100 pps Output
Corrected 1 kc Output
Corrected 10 kc Output
Corrected 100 kc Output
A13-TP1
500 usec One Shot A13
"OR" Gate A13
Corrected 100 pps Reference (Decimal "3") 10% Duty Cycle
100 pps Synthesized from VCO
OUTPUT DIVIDER CHAIN


50 to 10K Ohm Antenna Matching A1
R.F. Amplifier A1
30 Kc Lo-Pass Filter A1
0-80 db Attenuator A1
Buffer A1
Complementary Balanced Mixer A1
12.25 kc IF Amp. A1
Crystal Band-pass Filter 200 cps 2:1 80/3 db fo= 12.25 kc A1
1st IF Amp. A2
Emitter Follower A2
2nd IF Amp. A2
Emitter Follower A2
12.25 kc
A6-TP1
22.25 kc to 42.25 kc
Automatic Gain Control A2
Buffer A6
Emitter Follower Hi-Impedance A2
Integrator A2
AGC Amplifier A2
Relative Amplitude Monitor
÷ 2 Flip-Flop A6
R
T
100 pps from Synthesizer
A5-TP8
A5-TP7
A5-TP6
Inverter A5
Ambiguity Eliminate Gate A5
50 pps
÷ 2 Flip-Flop A5
T
Corrected 100 pps
2 Lines
4 Lines
4 Lines
A6-TP3
A6-TP4
180°
0°
Phase Splitter A6
A7-TP8
A8-TP8
Mod-10/Decimal Conversion Gates (Units Divisor) A7
Mod-10/Decimal Conversion Gates (Tens Divisor) A8
Mod-3 2 Flip-Flops (Hundreds Divisor
Voltage Controlled Oscillator 44.5 kc to 84.5 kc A6
10 Lines
10 Lines
3 Lines
Thumbwheel Frequency Selector Switch
Thumbwheel Frequency Selector Switch
Thumbwheel Frequency Selector Switch
Thumbwheel Switch and Resistance Network
A12-TP1
Inverter A12
Complementary Emitter Follower A12
Phase Detector A12
Integrator A12
Unity Gain Amplifier HI-Z A12
SYNTHESIZER PHASE DETECTOR (Slow Loop)
"OR" Gate A12
A13-TP3
A13-TP2
Emitter Follower A13
Unity Gain Amplifier (HI-Z) A13
Integrator A13
Sample and Hold Gate Phase Detector A13
Emitter Follower (HI-Z) A13
SYNTHESIZER PHASE DETECTOR (Fast Loop)




SERVO ASSEMBLY A2
SERVO PHASE DETECTOR
AGC PHASE DETECTOR
A15
CHOPPER
SERVO AMP
DEMODULATOR
MOTOR DRIVE
A18
DC SERVO MOTOR M
1KC
KC IF CT
C5 425UF NP
100KC
AGC
SERVO CUTOUT
A17
OFF ON
S8
TO AZ7C1
GEARS
DIGITAL COUNTER (USEC ACCU.)
M1
METER FUNCTION SWITCH S7
R1 AUDIO LEVEL 10K
AUDIO AMPLIFIER
A19
EXT REC
RECORDER
S10
TO 100 KC Ø SHIFTER
-12V
+12V
R5 499Ω P/O
R6 10K
R7 499Ω
CCW
CW
C1(POS)
XA20-31
XA20-30
E1
E2
A21,22,23,24,25,26 PIN 16
A17,18,19, PIN 16
A15,16, PIN 16
A14, PIN 16
A11,12,13, PIN 16
A5,7,8,9,10 PIN 16
A4 PIN 16
A3,4, PIN 16
A2 PIN 16
A1, PIN 8
AZ7R7
AZ7P5
A1, PIN 21
-12 BUS
+12 BUS
PWR SENSE
POWER SUPPLY
A20
Q3 2N1700
Q4 2N1702
Q1 2N1700
Q2 2N1702
R4 1K
R3 1K
C2 2000UF
C4 150 UF
C1 2000UF
C3 150UF
T1
40V 20V 0V
HUNDREDS DECIMAL CONVERSION GATES
245 FIXED COUNT GATE
VARIABLE COUNT GATE
CEP
RESET DRIVER
ONE SHOT
OR GATE
A10
RESET OUT
8 IN709A
CR1
XA5,7,8,9- PIN 24
76.8 TO 100KC CONVERTER
A24
LOCAL STD
J3
100KC
100KC PHASE (MOD-10)
A22
1KC TO 0.1KC DIVIDER (MOD-10)
A23
XA5-21
XA12-17
XA20-26
XA21-24
XA17-3 (100PPS MON.)
BUFFER
A25
DC-TO-DC CONVERTER
TB1
115V
F1 1/2A SB
S5
FL1
J10
P10
XA 17-11
XA17-28
*J10 IS PART OF FL 1.
TO SERVO MOTOR


RF AMPLIFIER MIXER XTAL FILTER
12.250KC IF AMP AGC AMP
AGC MONITOR
SECOND MIXER
3 FLIP-FLOPS AND GATES 45KC TO 11.250KC
50 PPS GATE
1KC IF AMP
SERVO PHASE DETECTOR AGC PHASE DETECTOR
CHOPPER SERVO AMP DEMODULATOR MOTOR DRIVE
DC SERVO MOTOR
SERVO ASSEMBLY
SERVO CUTOUT
DIGITAL COUNTER (USEC ACCU.)
AUDIO AMPLIFIER
METER FUNCTION SWITCH S7
RECORDER
EXT REC
UNITS DIVISOR (MOD-10)
TENS DIVISOR (MOD-10)
HUNDREDS DIVISOR
A FF INHIBIT
HUNDREDS DECIMAL CONVERSION GATES
345 FIXED COUNT GATE
VARIABLE COUNT GATE
RESET DRIVER
ONE SHOT
OR GATE
RESET OUT
SYNTHESIZER PHASE DETECTOR (SLOW LOOP)
SYNTH. PHASE DETECTOR (FAST LOOP)
THUMBWHEEL SWITCH ASSEMBLY A20
100 PPS GATE - 1/2 CYCLE OF VCO
100PPS REF.
VCO 44.5KC TO 84.5KC
AMP
OSC
76.8 TO 100KC CONVERTER
76.8/100 KC SWITCH
100KC INPUT AMP
100KC PHASE SHIFTER
100KC TO 10KC DIVIDER (MOD-10)
10KC TO 1KC DIVIDER (MOD-10)
1KC TO 0.1KC DIVIDER (MOD-10)
BUFFER
DC-TO-DC CONVERTER
POWER SUPPLY
ANTENNA
LOCAL STD
TO SERVO MOTOR
TO A27C1
GBAPS
*J10 IS PART OF FL 1.